

V:1.0

ECS
CONFIDENTIAL

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HSIO Lane Assignments by SKU (Lanes 1-14)

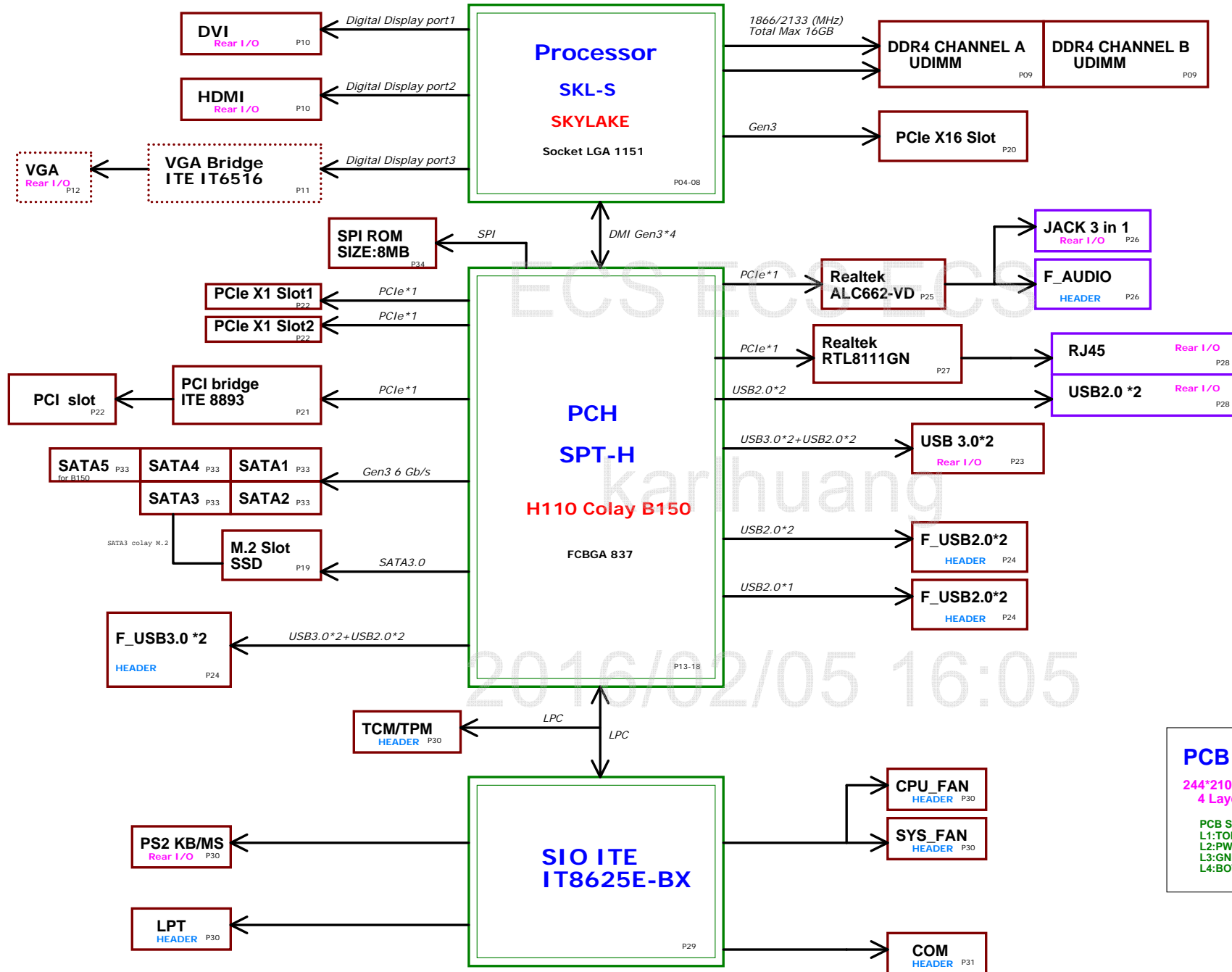
[illegible]

sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCle/LAN	PCle	PCle	PCle
B150	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCle/LAN	PCle	PCle	PCle
Q150	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	USB3	USB3	USB3	USB3	N/A	LAN Only	PCle/LAN	PCle	PCle	PCle
H170	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	USB3	USB3	USB3	USB3	PCle	PCle/LAN	PCle/LAN	PCle	PCle	PCle
Z170	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	USB3	USB3	USB3/PCle	USB3/PCle	USB3/PCle	USB3/PCle	PCle/LAN	PCle	PCle	PCle
Q170	USB3/OTG	USB3/SSIC	USB3/SSIC	USB3	USB3	USB3	USB3/PCle	USB3/PCle	USB3/PCle	USB3/PCle	PCle/LAN	PCle	PCle	PCle

HSIO Lane Assignments by SKU (Lanes 15-26)

	15	16	17	18	19	20	21	22	23	24	25	26	
	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16	PCIe #17	PCIe #18	PCIe #19	PCIe #20	
	SATA #0	SATA #1			SATA #0+*	SATA #1+*	SATA #2	SATA #3	SATA #4	SATA #5			
	QbE			QbE									
	X4			X4			X4			X4			
	X2		X2		X2		X2		X2		X2		
	Intel® RST for PCIe Storage				Intel® RST for PCIe Storage				Intel® RST for PCIe Storage				
Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Port
H110	PCIe/LAN	PCIe	N/A	LAN Only	SATA*/LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	
B150	PCIe/LAN	PCIe/SATA*	PCIe	PCIe/LAN	SATA*/LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A	
Q150	PCIe/LAN	SATA	PCIe	PCIe/LAN	PCIe/LAN/PCIe/SATA	SATA	SATA	PCIe/SATA	SATA	SATA	N/A	N/A	
H170	PCIe/LAN	SATA	PCIe	PCIe/LAN	PCIe/LAN/PCIe/SATA	SATA	PCIe/SATA	PCIe/SATA	SATA	SATA	PCIe	PCIe	
Z170	PCIe/LAN	PCIe	PCIe	PCIe/LAN	PCIe/LAN/PCIe/SATA	SATA	PCIe/SATA	PCIe/SATA	PCIe/SATA	PCIe/SATA	2PCIe	PCIe	
Q170	PCIe/LAN	SATA	PCIe	PCIe/LAN	PCIe/LAN/PCIe/SATA	SATA	SATA	PCIe/SATA	PCIe/SATA	PCIe/SATA	PCIe	PCIe	

Skylake-S Desktop Platform



PCB SIZE

244*210*1.6mm
4 Layers

PCB STACK:
L1:TOP
L2:PW/R
L3:GND
L4:BOTTOM

PCH-GPIO function

Pin Name	Power Well	Usage	Boot Set
GPP_A11	3VSB	LPC_PME_L	PME#
GPP_B13	3VSB	PCH_PLTRST_L	PLTRST#
GPP_G13	VCC3	HDPANEL_DETECT	GPI
GPP_E8	VCC3	SATALED_L	SATALED#
GPP_B14	VCC3	PCH_SPKR	SPKR
GPP_A14	3VSB	LPCPD_L	SUS_STAT#
GPP_C6	3VSB	SML1_CLK	SML1CLK
GPP_C7	3VSB	SML1_DATA	SML1DATA

SIO-GPIO function

Pin Name	Power Well	Usage	Default SET
PCH_D0B/GP22	+ATX3VSB	SIO_LED0	GPO
PCIRST3#/GP10/CIRRX1	+ATX3VSB	SIO_LED1	GPO
GP92/GP93/GP94	+ATX3VSB	BOM selection	GPI

Interrupt mapping

Function	INT# port	PCIe*1 port	Device
LAN	INTB#	Port 6	RTL8111GN
SATA	INTA#	NA	SATA3.0
PCIeX1 slot1	INTA#	Port 5	PCIE device
PCIeX1 slot2	INTC#	Port 7	PCIE device
PCI	INTB#	Port 8	PCI device

Change List

- P07 CPU-PWR
chabged TP ref. name form +VCORE1 to VCCIO_SENSE
- P14 SIO-IT8625E
removed TP10 & connected SIO_SLP_SUS# to PCH_SLP_SUS#
- P23 USB3.0 CONN
removed C50
- P24 USB2.0/USB3.0 Header
removed C488,C508,C644
- P31 LPT/COM/PS2
added R1,R2,R3,R4 short pad for EMI request
- P38 DC/DC VCCIO
added LDO_VCCIO
connected VR_ENABLE to VCORE & VCCSA
- P39 DC/DC VDIMM/TT/VP
removed C547
connected VDDQ_PWRGD to LDO_VCCIO
- P40 DC/DC 5VDUAL/SEQUENCE
removed C298,C299,C561,C581,C593,R658,

DDR4 CH.A

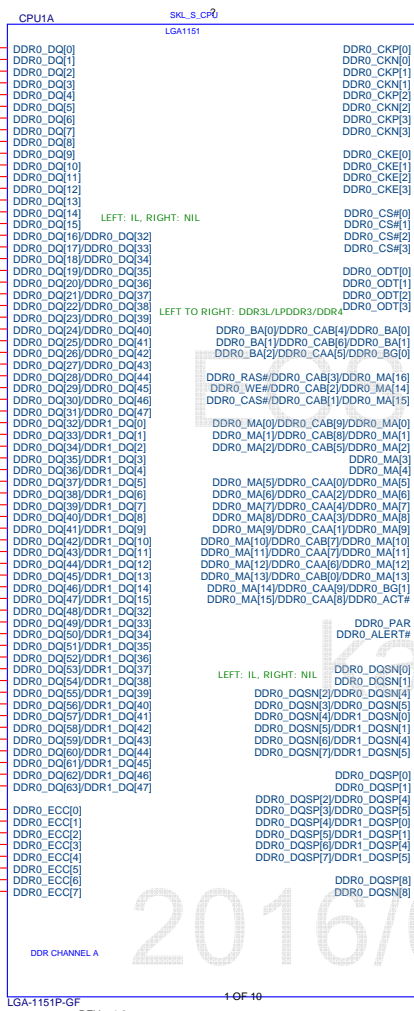
<-> M_DQS_A_P[0..8] <-> M_DQS_A_N[0..8]
 <-> M_DATA_A[0..63] <-> M_DATA_A_CB[0..7]
 <-> M_ODT_A[0..1] <-> M_ODT_A[0..1]
 <-> M_CKE_A[0..1] <-> M_CS_A_L[0..1]
 <-> M_CLK_A_P[0..1] <-> M_CLK_A_N[0..1]
 <-> M_MA_A[0..16] <-> M_MA_A[0..16]

DDR4 CH.B

<-> M_DQS_B_P[0..8] <-> M_DQS_B_N[0..8]
 <-> M_DATA_B[0..63] <-> M_DATA_B_CB[0..7]
 <-> M_ODT_B[0..1] <-> M_ODT_B[0..1]
 <-> M_CKE_B[0..1] <-> M_CS_B_L[0..1]
 <-> M_CLK_B_P[0..1] <-> M_CLK_B_N[0..1]
 <-> M_MA_B[0..16] <-> M_MA_B[0..16]

Follow DDR4 RVP8 CRB

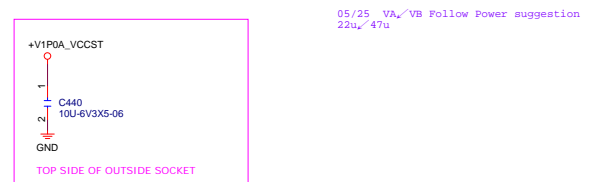
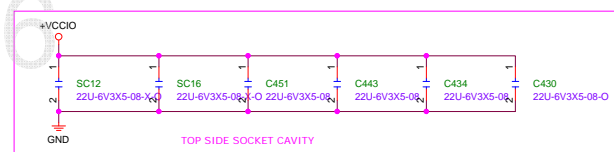
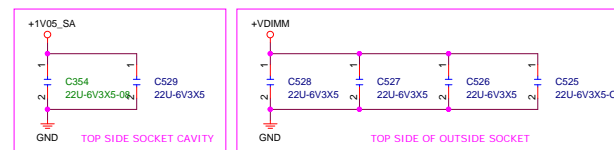
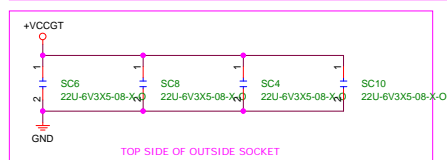
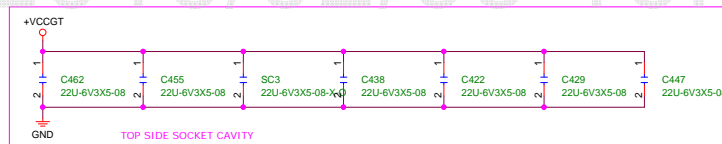
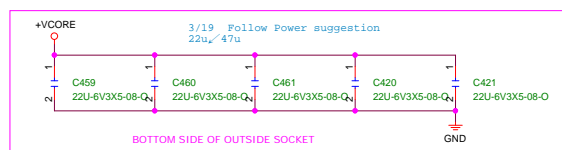
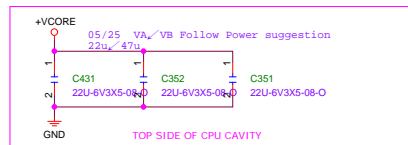
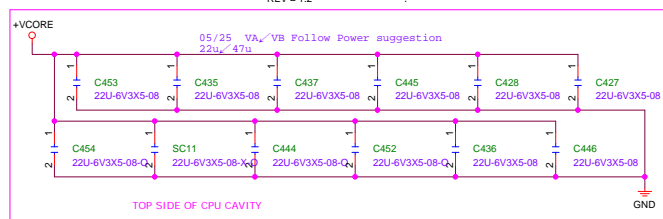
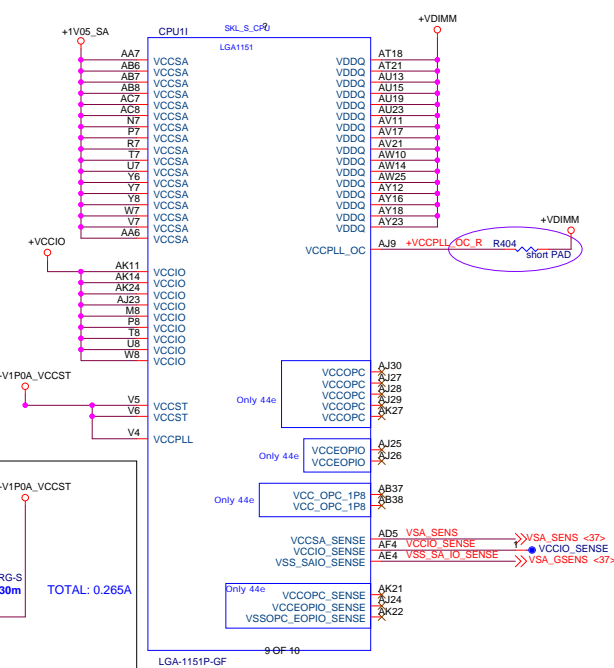
**Attention

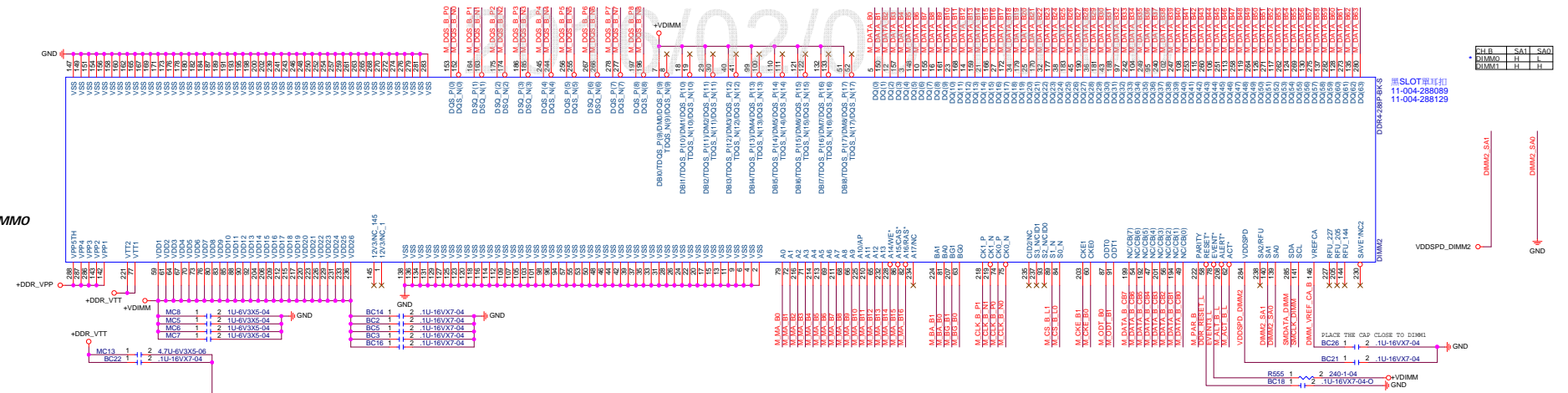
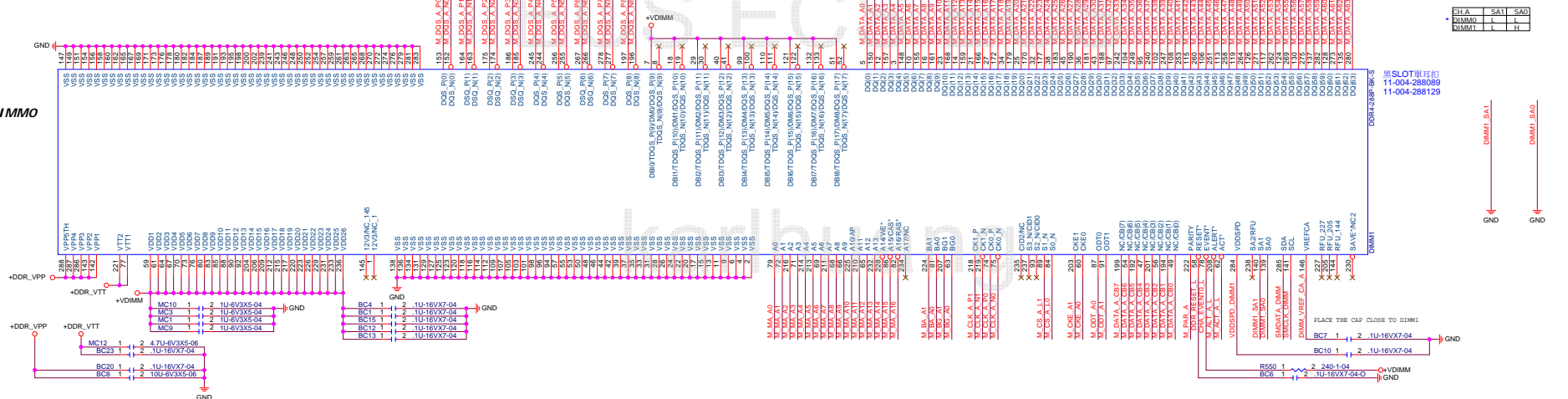
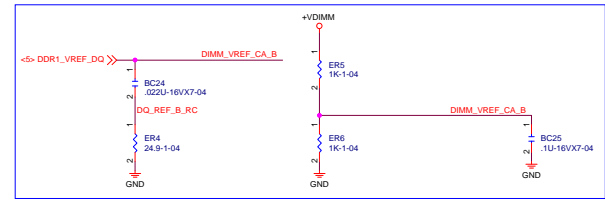
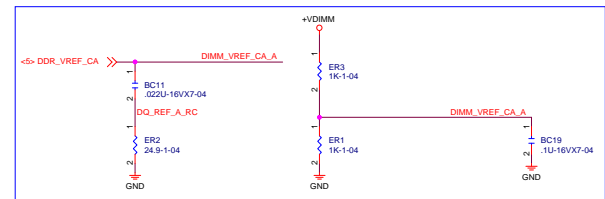
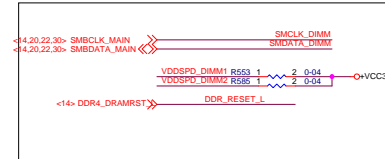
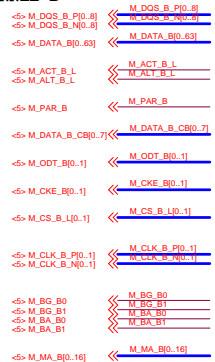
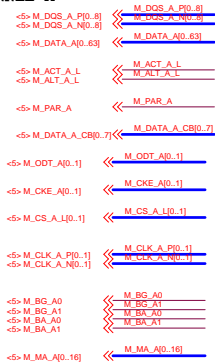


Follow DDR4 RVP8 CRB

**Attention



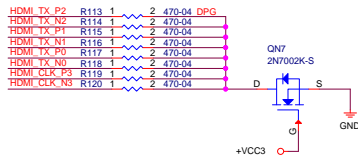




Port 2	DDI2_TXP[0]	DDI2_LANE0_DP	HDMIx_TX2_DP
	DDI2_TXN[0]	DDI2_LANE0_DN	HDMIx_TX2_DN
	DDI2_TXP[1]	DDI2_LANE1_DP	HDMIx_TX1_DP
	DDI2_TXN[1]	DDI2_LANE1_DN	HDMIx_TX1_DN
	DDI2_TXP[2]	DDI2_LANE2_DP	HDMIx_TX0_DP
	DDI2_TXN[2]	DDI2_LANE2_DN	HDMIx_TX0_DN
	DDI2_TXP[3]	DDI2_LANE3_DP	HDMIx_CLK_DP
	DDI2_TXN[3]	DDI2_LANE3_DN	HDMIx_CLK_DN

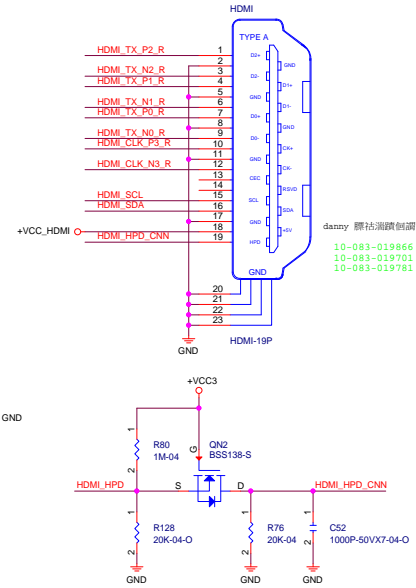
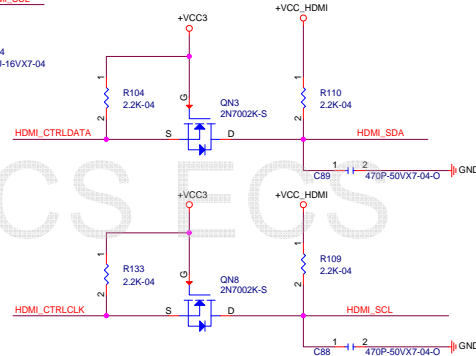
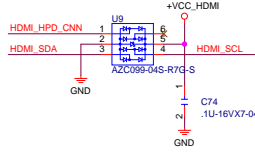
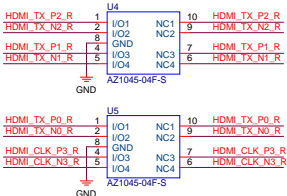
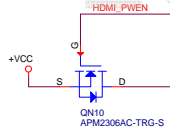
HDMI

HDMI的DDI_TX信號, TX0和TX2必須交換1次			
<4> DDI2_TX_P0	C117 1	2	1U-16VX7-04
<4> DDI2_TX_N0	C118 1	2	1U-16VX7-04
<4> DDI2_TX_P1	C119 1	2	1U-16VX7-04
<4> DDI2_TX_N1	C120 1	2	1U-16VX7-04
<4> DDI2_TX_P2	C121 1	2	1U-16VX7-04
<4> DDI2_TX_N2	C122 1	2	1U-16VX7-04
<4> DDI2_TX_P3	C123 1	2	1U-16VX7-04
<4> DDI2_TX_N3	C124 1	2	1U-16VX7-04



HDMI_TX_P2	HDMI_TX_P2_R
HDMI_TX_N2	HDMI_TX_N2_R
HDMI_TX_P1	HDMI_TX_P1_R
HDMI_TX_N1	HDMI_TX_N1_R

HDMI_TX_P0	HDMI_TX_P0_R
HDMI_TX_N0	HDMI_TX_N0_R
HDMI_CLK_P3	HDMI_CLK_P3_R
HDMI_CLK_N3	HDMI_CLK_N3_R



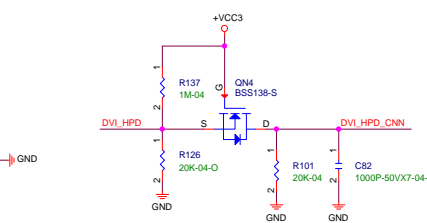
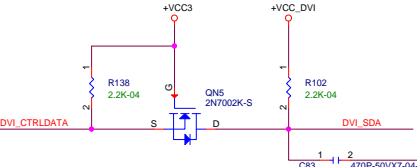
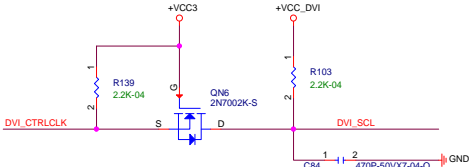
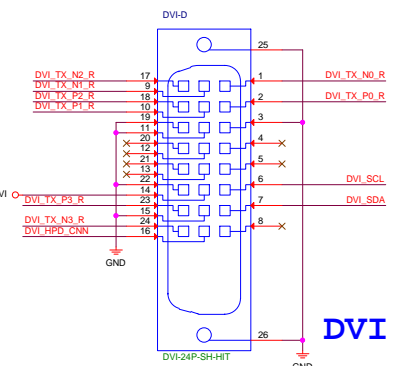
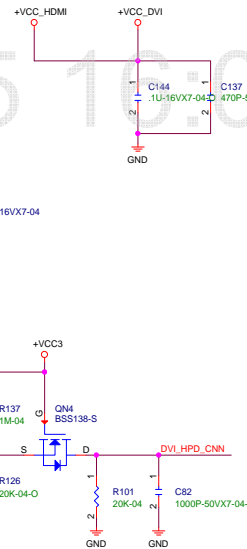
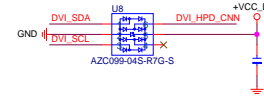
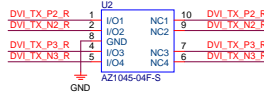
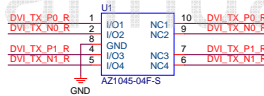
DVI

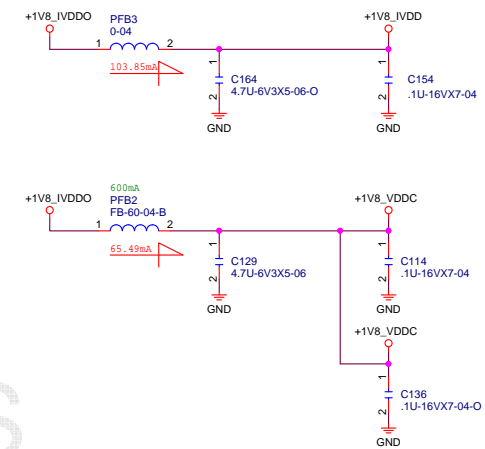
<4> DDI1_TX_P0	C35 1	2	1U-16VX7-04
<4> DDI1_TX_N0	C36 1	2	1U-16VX7-04
<4> DDI1_TX_P1	C37 1	2	1U-16VX7-04
<4> DDI1_TX_N1	C38 1	2	1U-16VX7-04
<4> DDI1_TX_P2	C39 1	2	1U-16VX7-04
<4> DDI1_TX_N2	C40 1	2	1U-16VX7-04
<4> DDI1_TX_P3	C41 1	2	1U-16VX7-04
<4> DDI1_TX_N3	C42 1	2	1U-16VX7-04



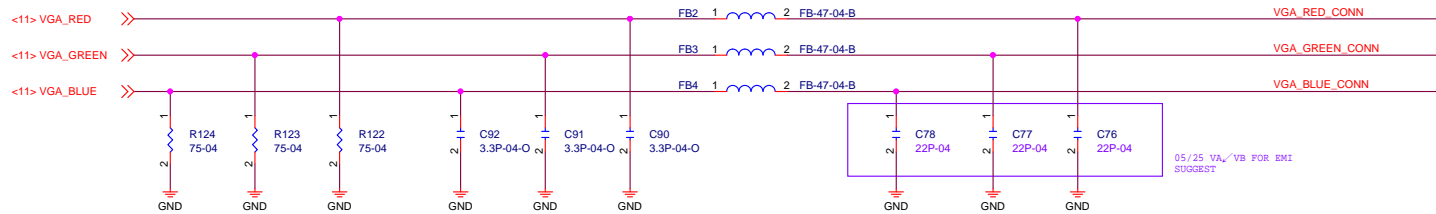
DVI_TX_P0	DVI_TX_P0_R
DVI_TX_N0	DVI_TX_N0_R
DVI_TX_P1	DVI_TX_P1_R
DVI_TX_N1	DVI_TX_N1_R

DVI_TX_P2	DVI_TX_P2_R
DVI_TX_N2	DVI_TX_N2_R
DVI_TX_P3	DVI_TX_P3_R
DVI_TX_N3	DVI_TX_N3_R

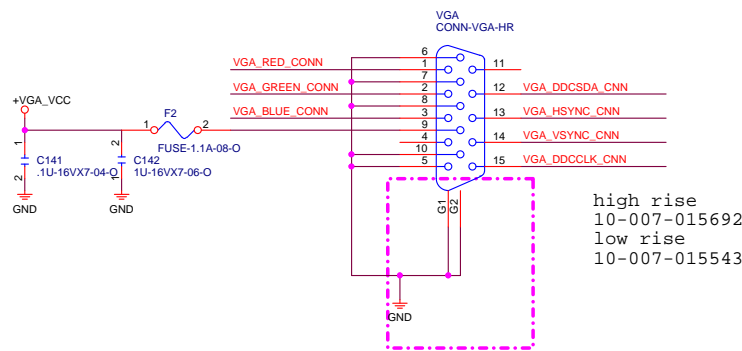
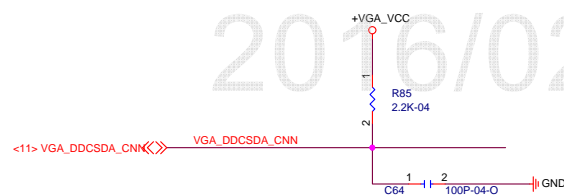
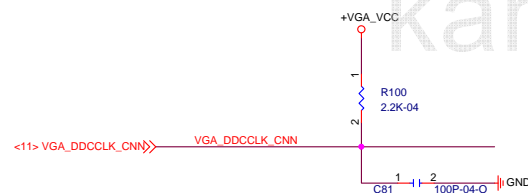
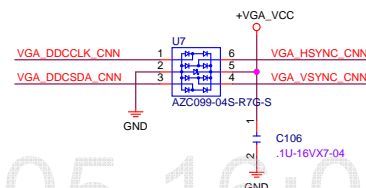
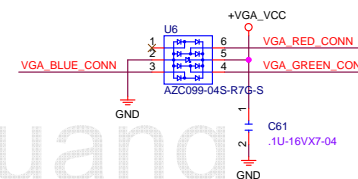
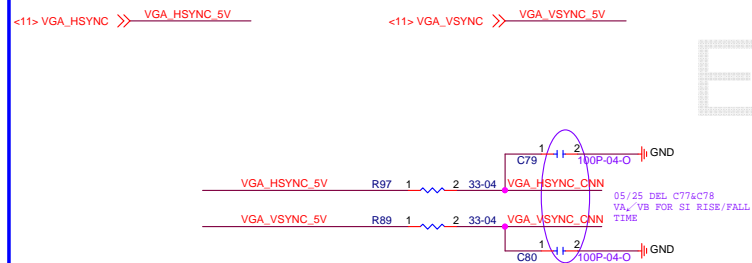


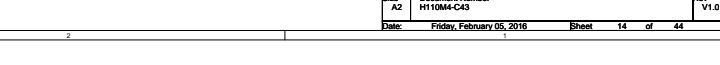
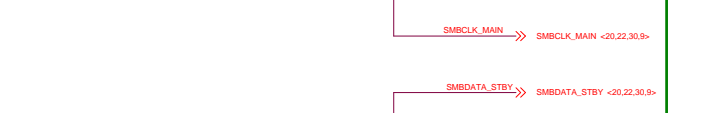
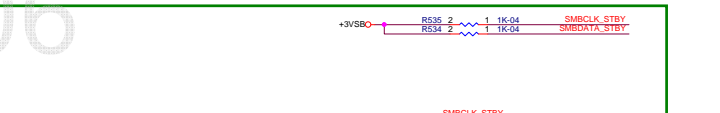
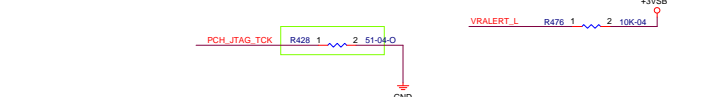
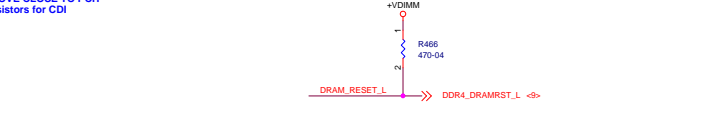
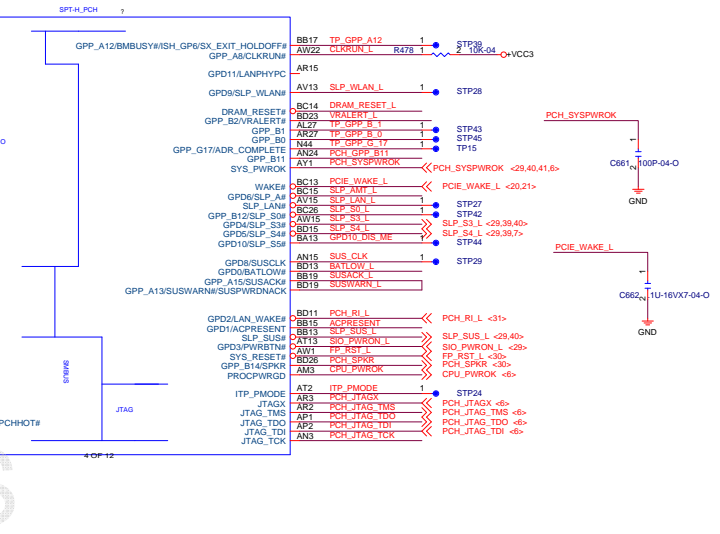
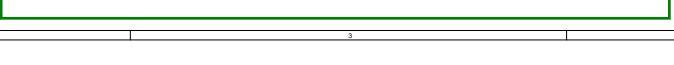
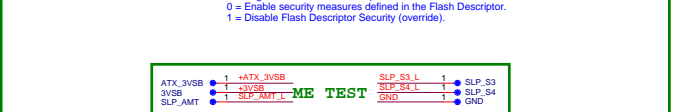
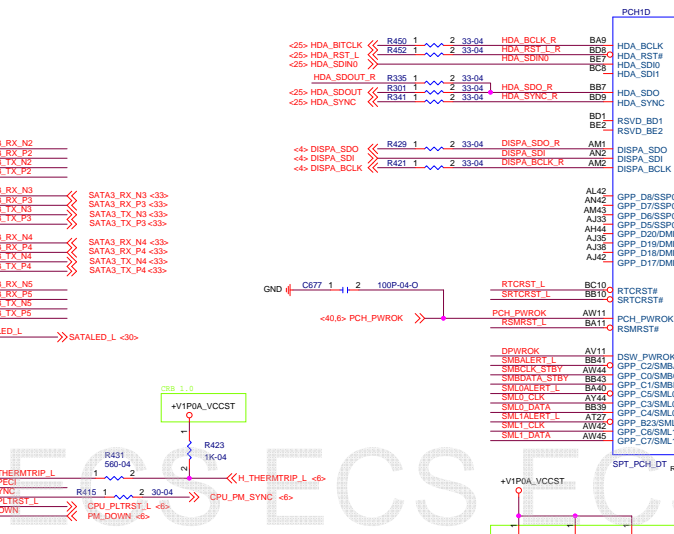
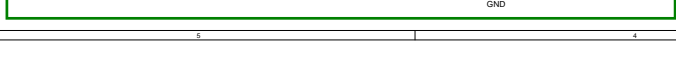
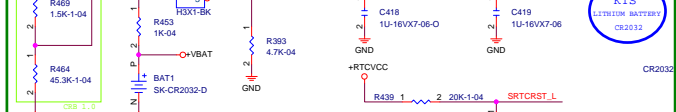
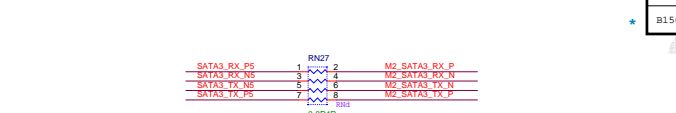
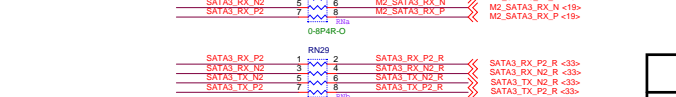
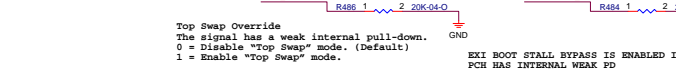
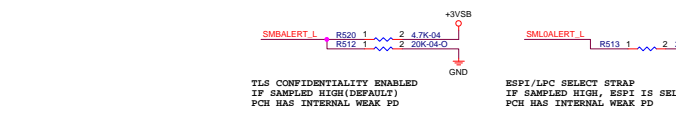
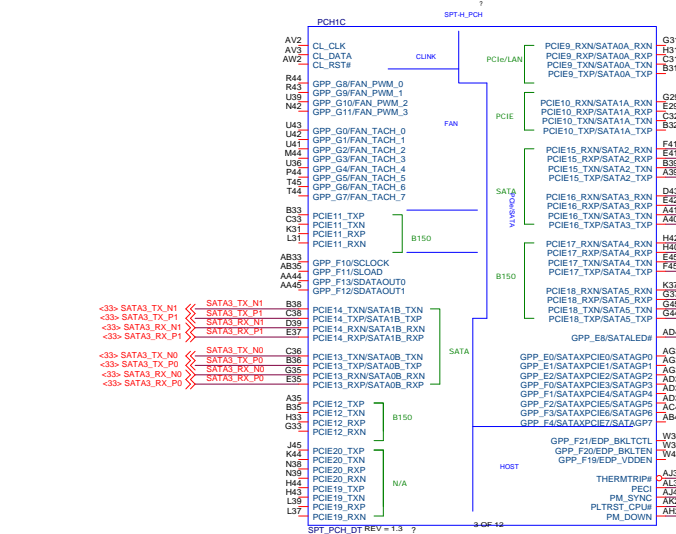


VGA



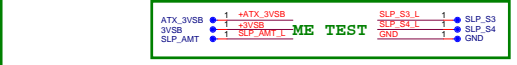
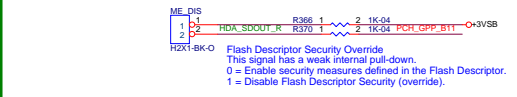
Level shifter,default 0 ohm



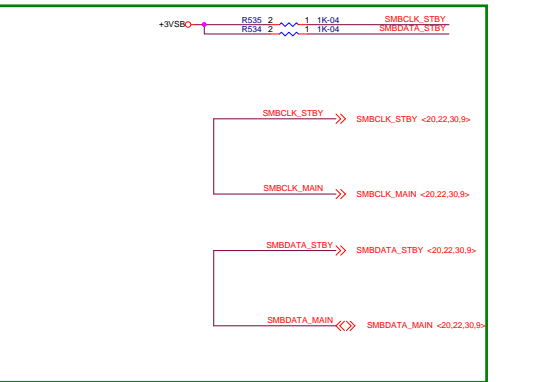
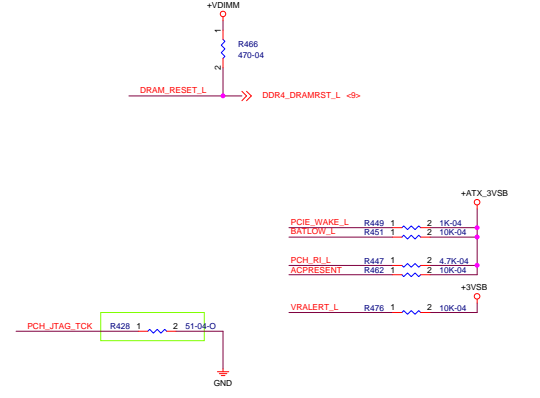


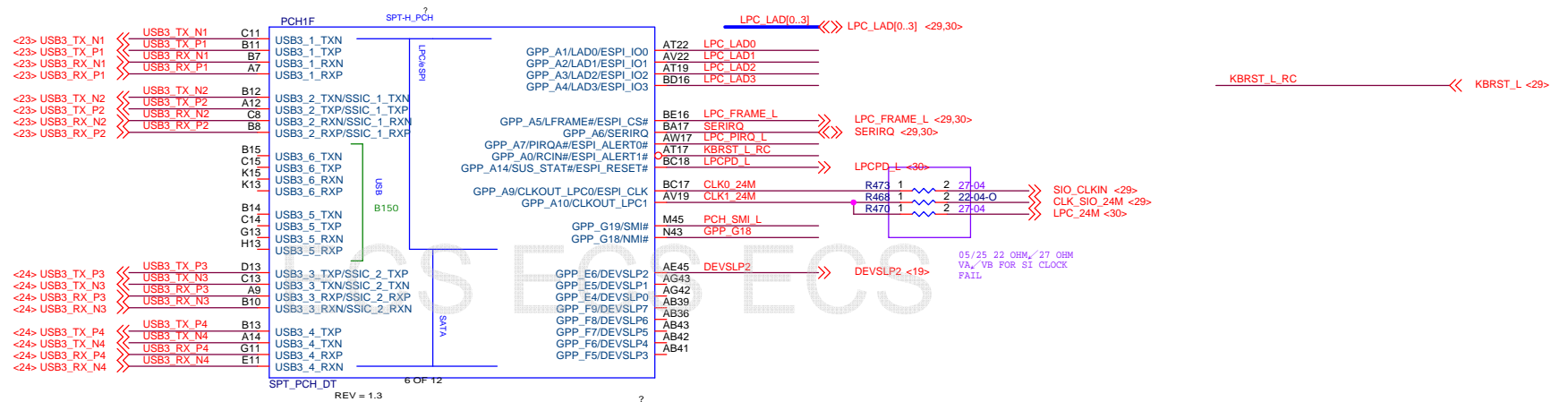
	RNa	RNb	RNd
H110(3 SATA + M.2)	V	X	X
H110(4 SATA)	X	V	X
H150(5 SATA + M.2)	X	V	V

ME disable

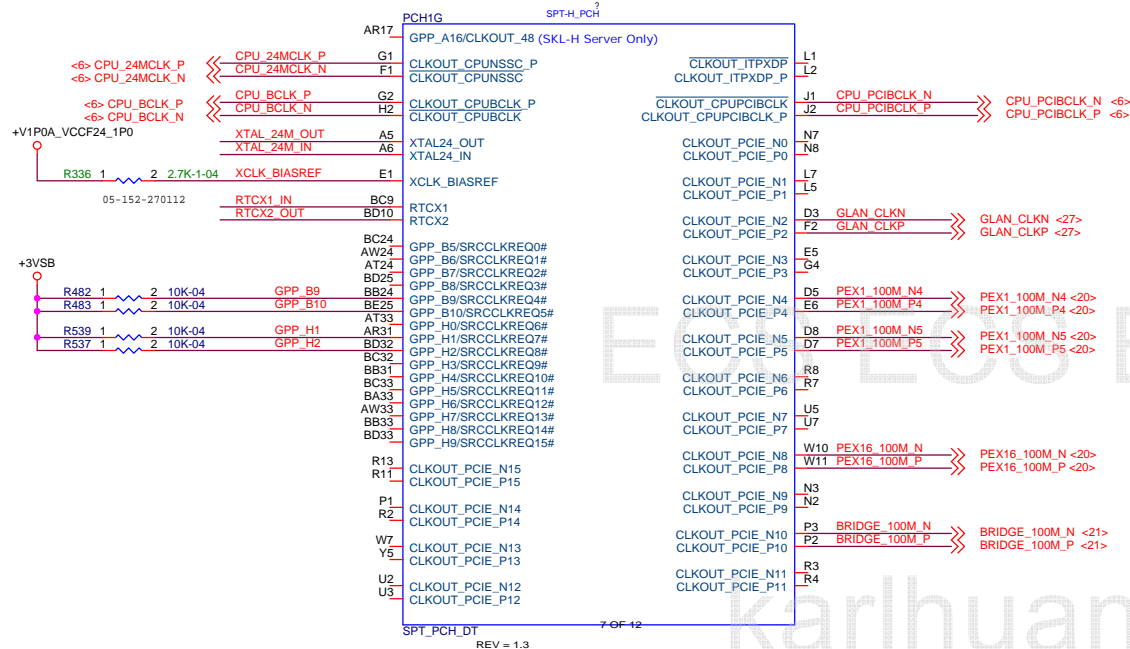


DDR4_DRAMRST



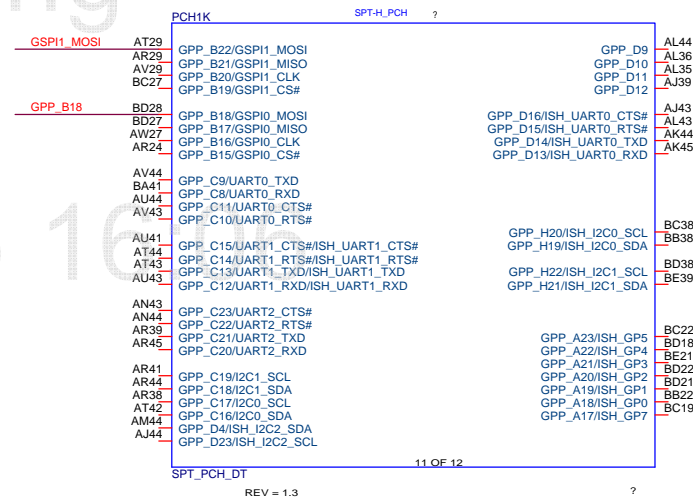
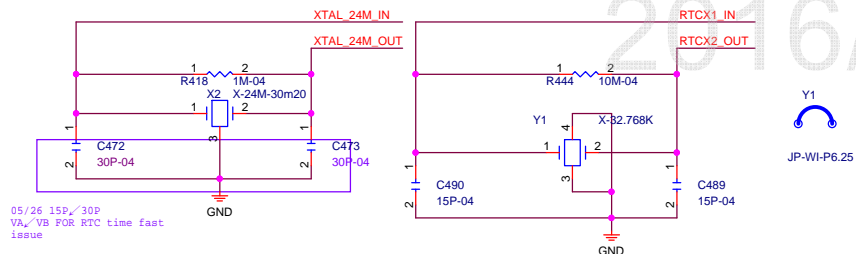


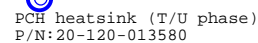
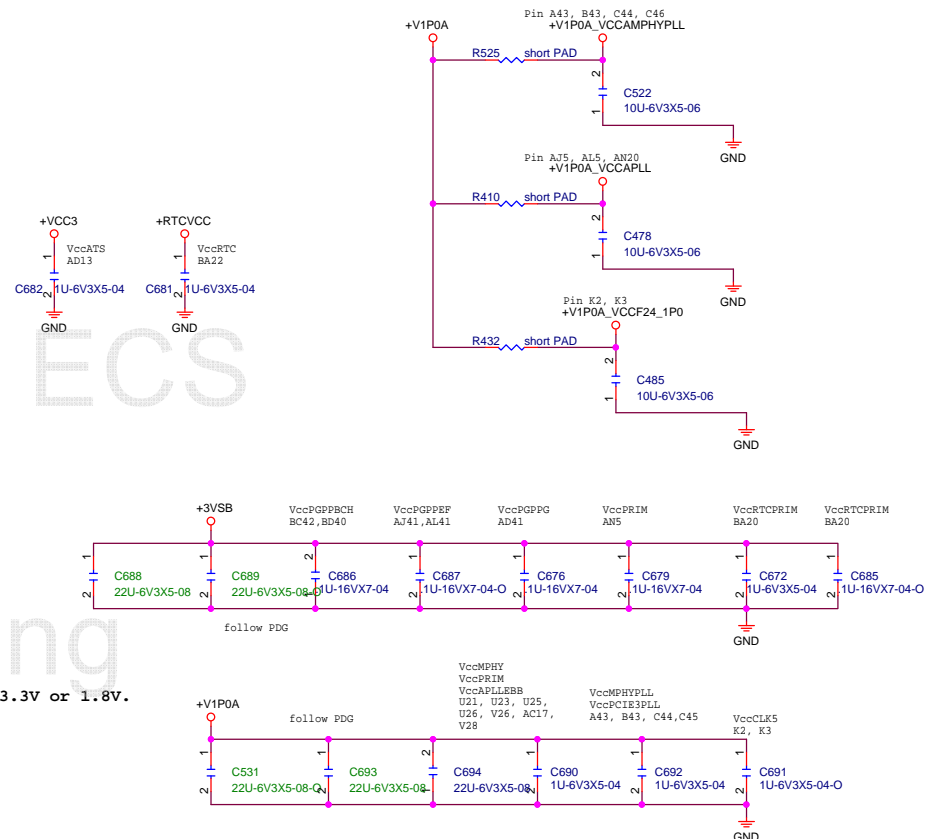
follow PDG eDP Disabling need Pull down to ground via 100k ohm resistor



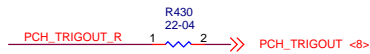
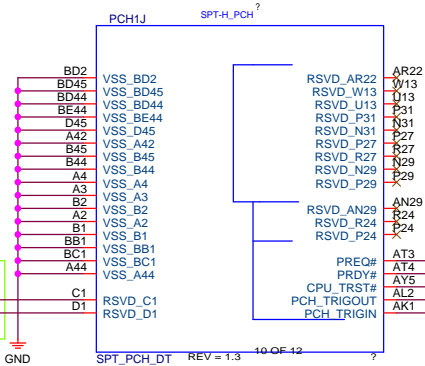
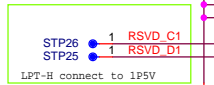
BOOT SELECT STRAP
IF SAMPLED HIGH, LPC IS SELECTED ELSE SPI
PCH HAS INTERNAL WEAK PD

NO REBOOT IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD

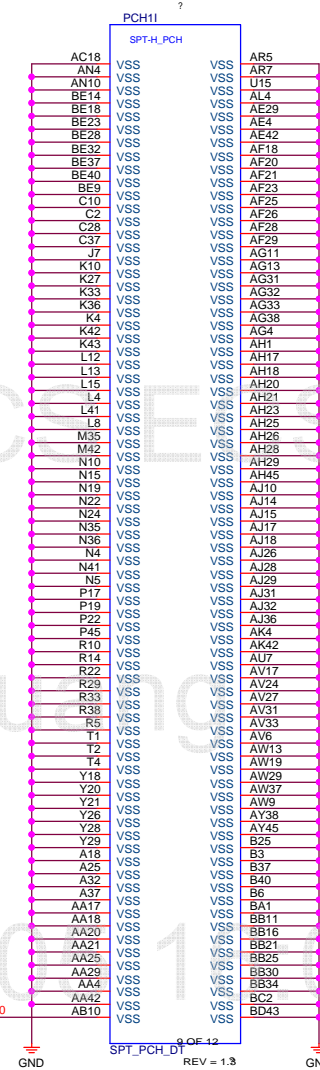




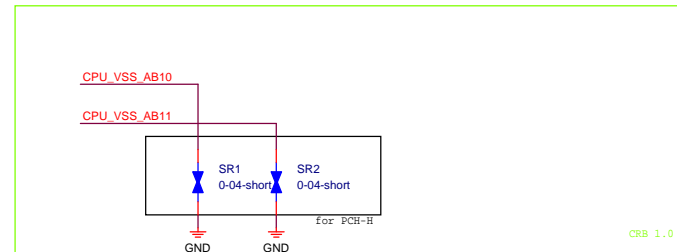
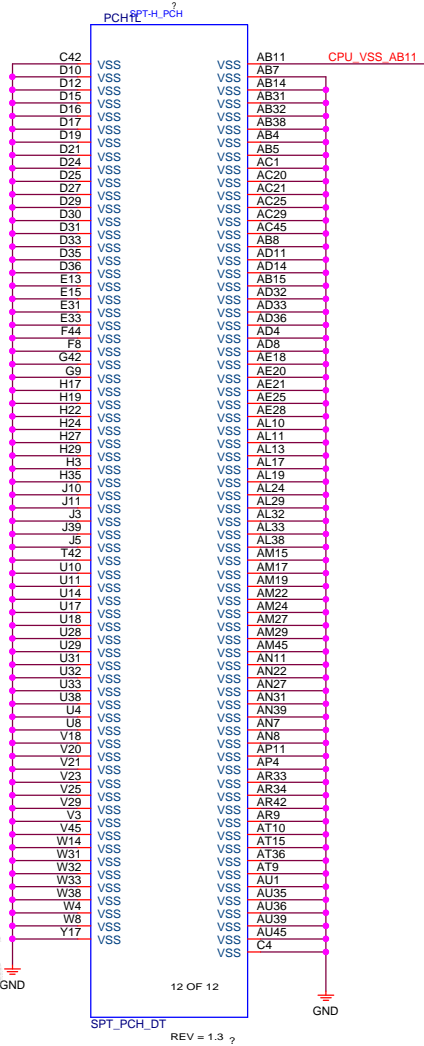
CRB 1.0

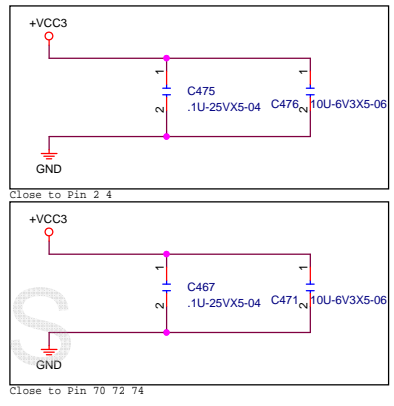
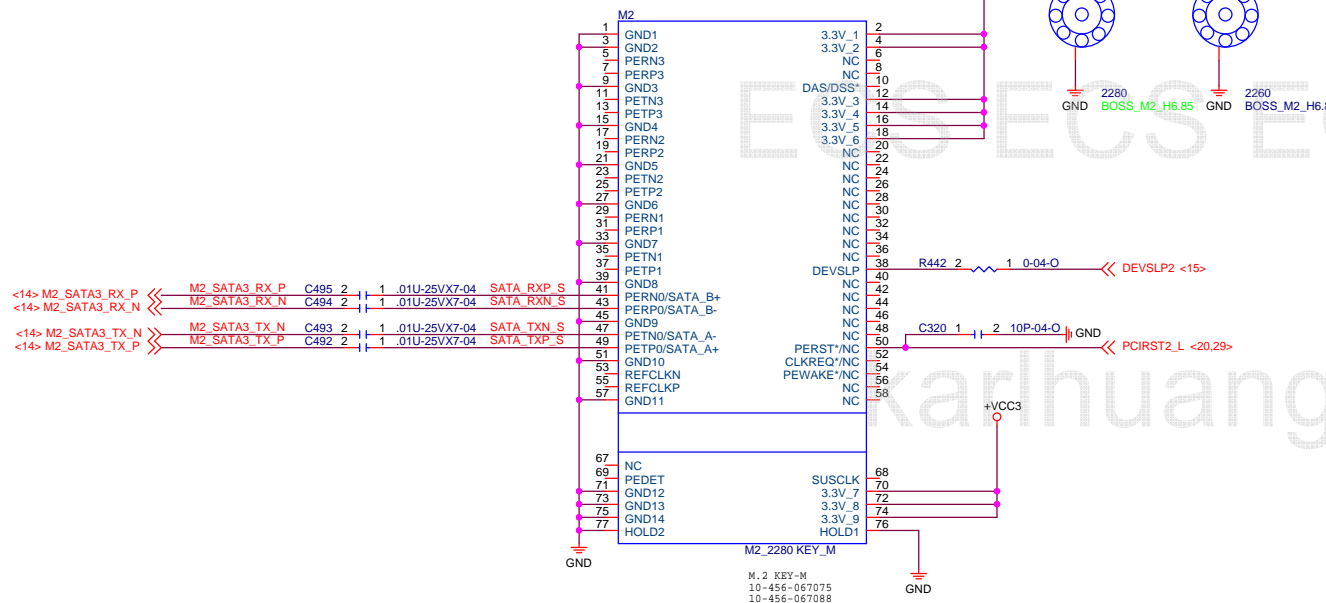


CPU_VSS_AB10

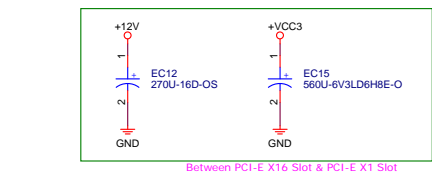


CPU_VSS_AB10

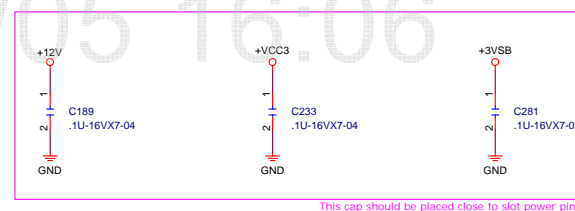
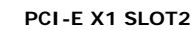




PCI-E SPEC
VCC3:3A
12V:5.5A
3VSB:0.375A



Between PCI-E X16 Slot & PCI-E X1 Slot



This cap should be placed close to slot power pin

<21> AD[31..0] <<> AD[31..0]
 <21> C_BE_L[3..0] <<> C_BE_L[3..0]

<21> GNT0_L <<> GNT0_L
 <21> REQ0_L <<> REQ0_L

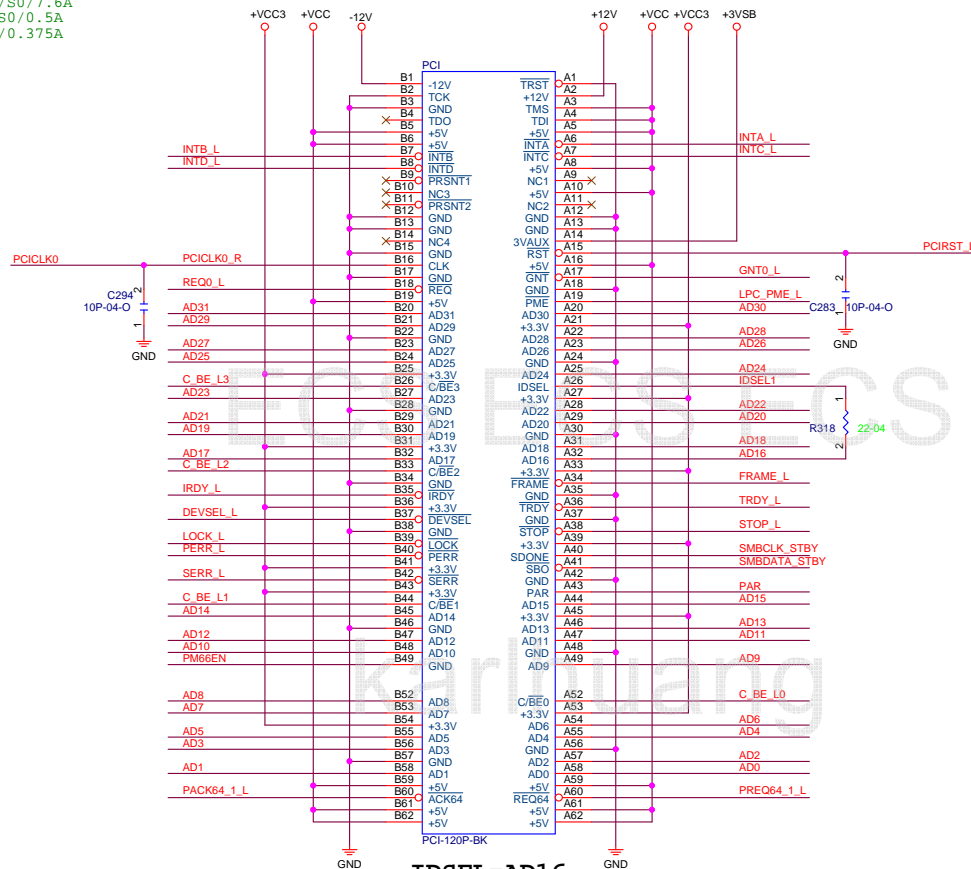
<21> INTA_L <<> INTA_L
 <21> INTB_L <<> INTB_L
 <21> INTC_L <<> INTC_L
 <21> INTD_L <<> INTD_L

<21> PAR <<> PAR
 <21> DEVSEL_L <<> DEVSEL_L
 <21> IRDY_L <<> IRDY_L
 <13,29> LPC_PME_L <<> LPC_PME_L
 <21> SERR_L <<> SERR_L
 <21> STOP_L <<> STOP_L
 <21> LOCK_L <<> LOCK_L
 <21> TRDY_L <<> TRDY_L
 <21> PERR_L <<> PERR_L
 <21> FRAME_L <<> FRAME_L

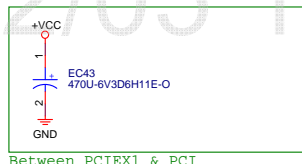
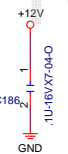
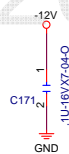
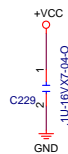
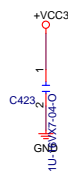
<21> PCIRST_L <<> PCIRST_L
 <21> PCICLK0 <<> PCICLK0
 <21> PCICLK0 <<> PCICLK0
 <21> PM66EN <<> PM66EN

<14,20,30,9> SMBCLK_STBY <<> SMBCLK_STBY
 <14,20,30,9> SMBDATA_STBY <<> SMBDATA_STBY

PCI Slot
 +VCC/S0/5A
 +VCC3/S0/7.6A
 +V12/S0/0.5A
 +3VSB/0.375A



IDSEL=AD16
 INT[A,B,C,D]



<13> USB_N1 <<> USB_N1
<13> USB_P1 <<> USB_P1

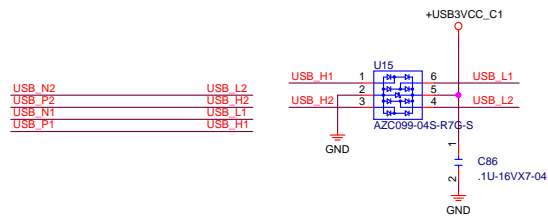
<13> USB_N2 <<> USB_N2
<13> USB_P2 <<> USB_P2

<15> USB3_TX_P1 >> C152 1 2 .1U-16VX7-04 USB3_TX_P1_C
<15> USB3_TX_N1 >> C151 1 2 .1U-16VX7-04 USB3_TX_N1_C

<15> USB3_TX_P2 >> C150 1 2 .1U-16VX7-04 USB3_TX_P2_C
<15> USB3_TX_N2 >> C149 1 2 .1U-16VX7-04 USB3_TX_N2_C

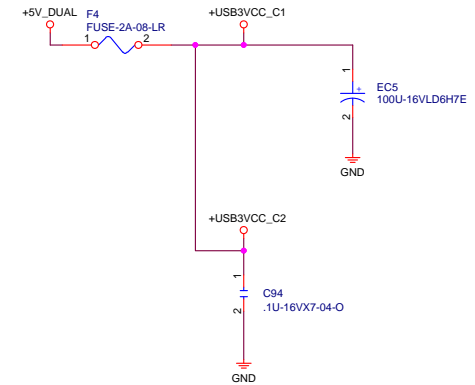
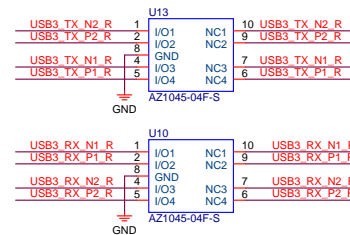
<15> USB3_RX_P1 <<> USB3_RX_P1
<15> USB3_RX_N1 <<> USB3_RX_N1

<15> USB3_RX_P2 <<> USB3_RX_P2
<15> USB3_RX_N2 <<> USB3_RX_N2

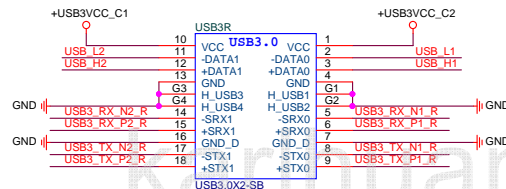


USB3_TX_N2_C USB3_TX_N2_R
USB3_TX_P2_C USB3_TX_P2_R
USB3_TX_N1_C USB3_TX_N1_R
USB3_TX_P1_C USB3_TX_P1_R

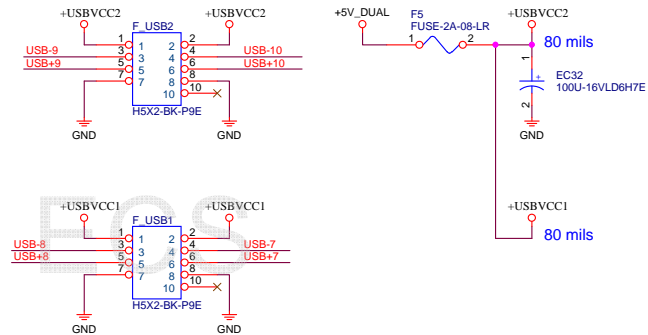
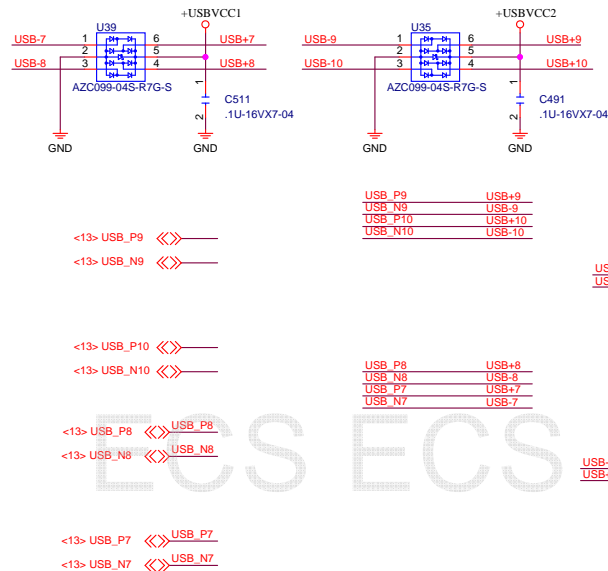
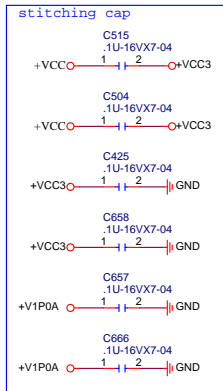
USB3_RX_N1 USB3_RX_N1_R
USB3_RX_P1 USB3_RX_P1_R
USB3_RX_N2 USB3_RX_N2_R
USB3_RX_P2 USB3_RX_P2_R



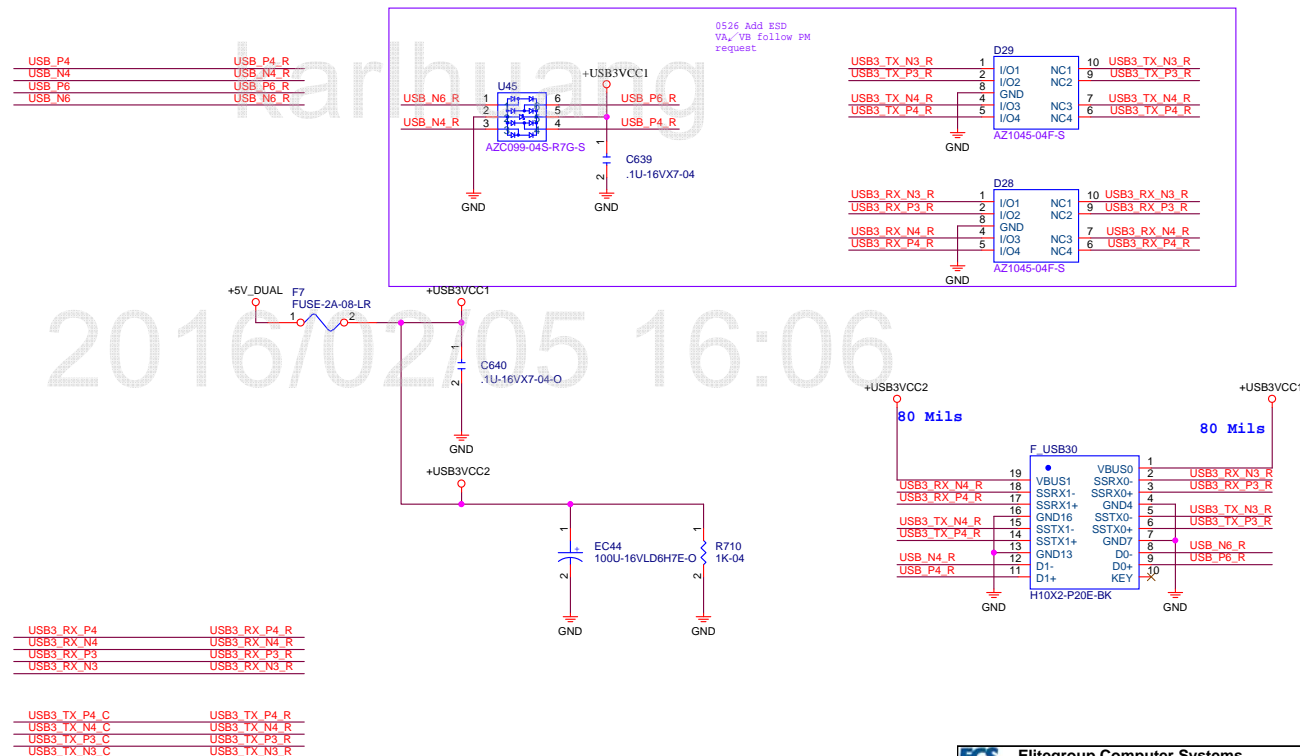
Dual USB3.0 PORT



LOTS: 10-084-018062
HI-TOP : 10-084-018690



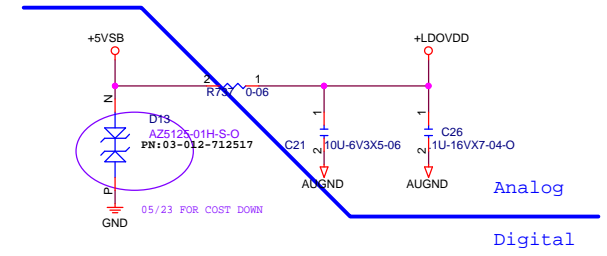
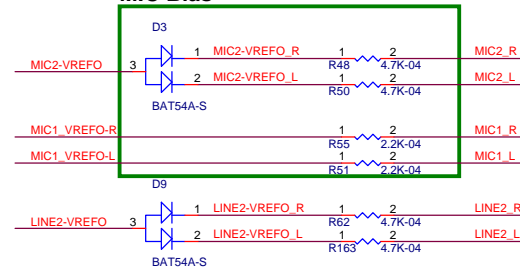
USB2.0 header



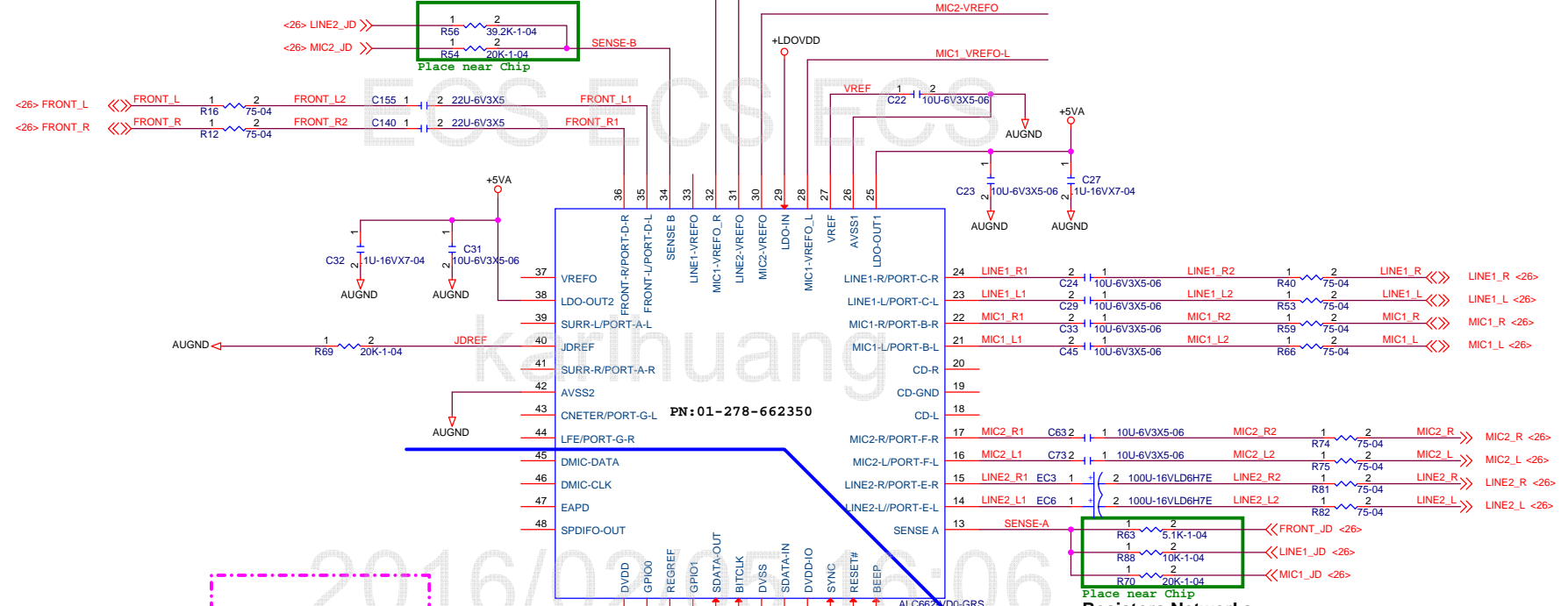
USB3.0 header

Elitegroup Computer Systems			
USB2.0/USB3.0 Header			
Size	Document Number	Rev	
Custom	H110M4-C43	V1.0	
Date:	Friday, February 05, 2016	Sheet	24 of 44

MIC Bias

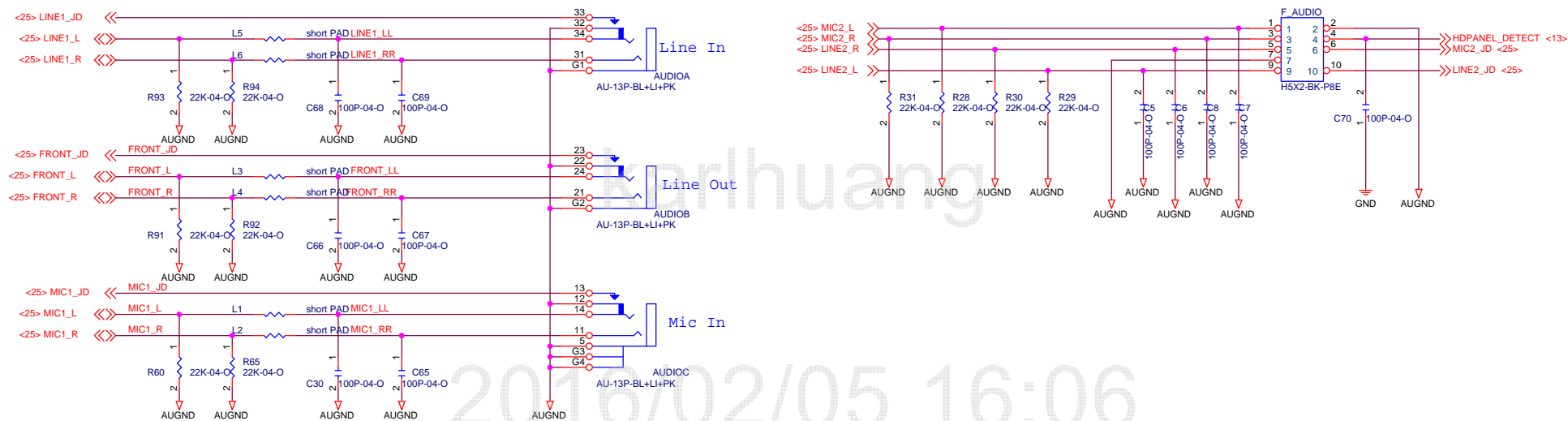


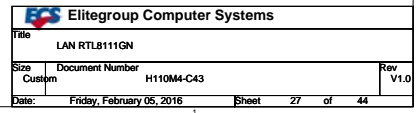
Resistors Networks

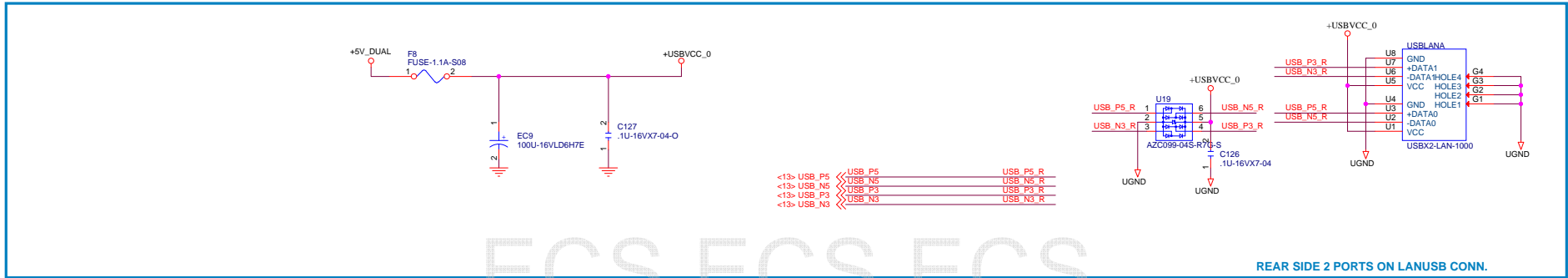


Resistors Networks

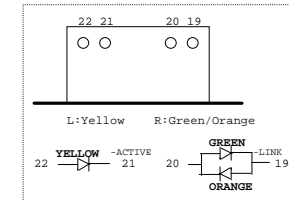
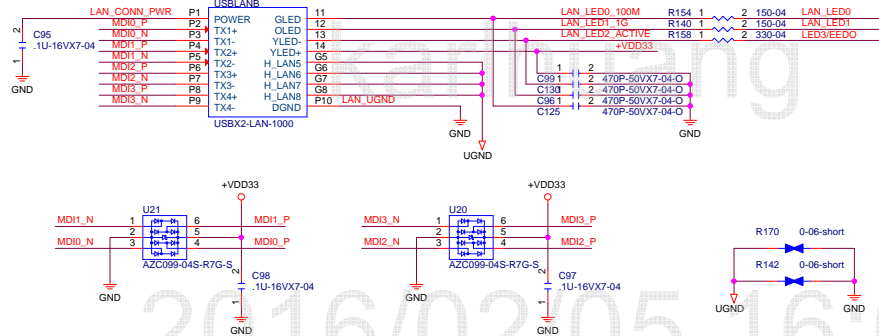
Analog
Digital







<27> LAN_LED0 >> LAN_LED0
 <27> LAN_LED1 >> LAN_LED1
 <27> LED3/EED0 >> LED3/EED0
 <27> MDI0_P >> MDI0_P
 <27> MDI0_N >> MDI0_N
 <27> MDI1_P >> MDI1_P
 <27> MDI1_N >> MDI1_N
 <27> MDI2_P >> MDI2_P
 <27> MDI2_N >> MDI2_N
 <27> MDI3_P >> MDI3_P
 <27> MDI3_N >> MDI3_N



For China-one LED Light:

LAN LED Behavior		
Status	Yellow	Grn/Org
No Link	Off	Off
S3/S4/S5	Off	Off
10M inactive	Off	Off
10M active	Off	Off
100M inactive	Off	Off
100M active	Off	Off
1G inactive	Off	Off
1G active	Off	Off
Blinking	Off	Off

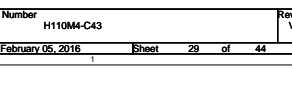
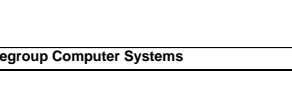
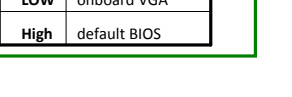
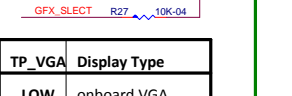
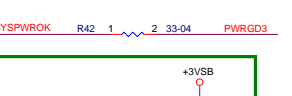
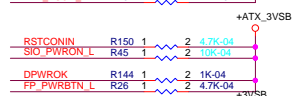
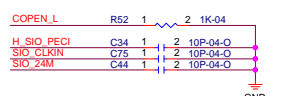
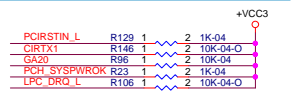
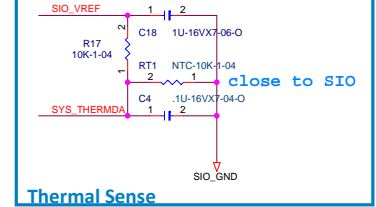
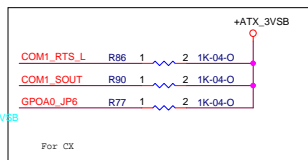
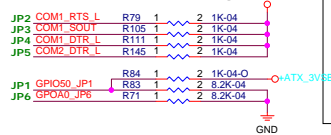
7. Power On Strapping Options and Special Pin Routings

Table 7-1. Power On Strapping Options

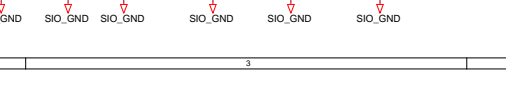
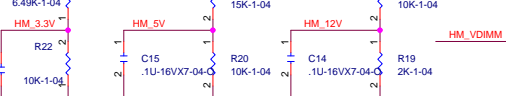
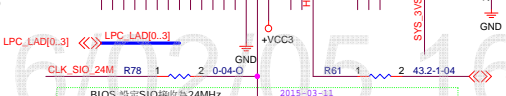
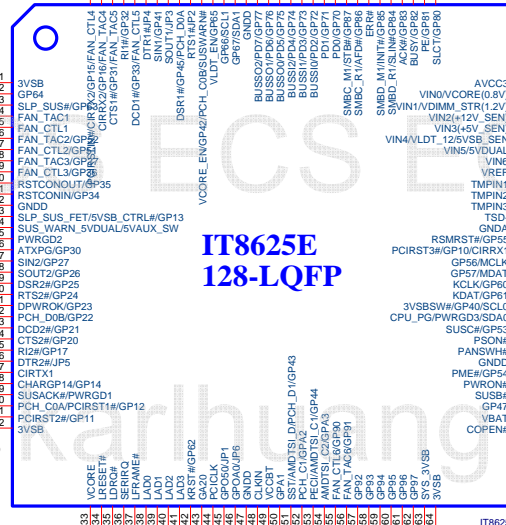
Symbol	Strapping Event	Value	Description
Jp1 Pin 45	DSW_EUP_SEL	Internal 3VSB_OK	1 EUP
Jp2 Pin 119	WDT_EN	Internal VCC-OK/ LRESET#	0 DS#
Jp3 Pin 121	FAN_CTL_SEL	Internal VCC-OK	1 The default value of EC Index 63h/68h/73h/7Bh/A3h/ABh is 80h.
Jp4 Pin 123	KBPWR_EN	Internal VCC-OK	0 The default value of EC Index 63h/68h/73h/7Bh/A3h/ABh is 00h.
Jp5 Pin 28	UOVMODE_SEL	Internal VCC-OK	1 Notice Type
Jp6 Pin 46	Vin/Vii_SEL	Internal VCC-OK	0 Force-Type
			0 Not Bay-Trail Platform

Note:
1. Pull-down with 8.2k ohm recommended.
2. This function must be pulled up to 3VSB.
3. 1.8V input threshold voltage for SUS#SUSC#LRESET#SERIRQ#GP2x signals.
3.3V input threshold voltage for SUS#SUSC#LRESET#SERIRQ#GP2x signals.

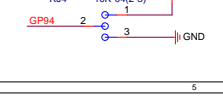
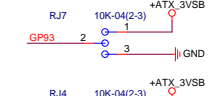
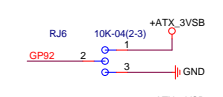
Power On Strapping



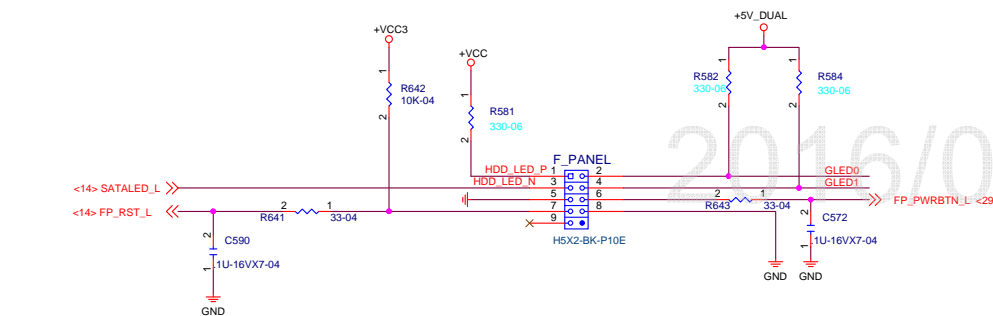
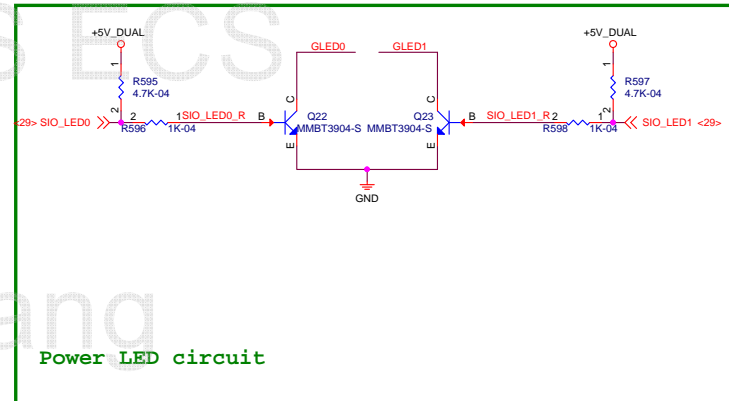
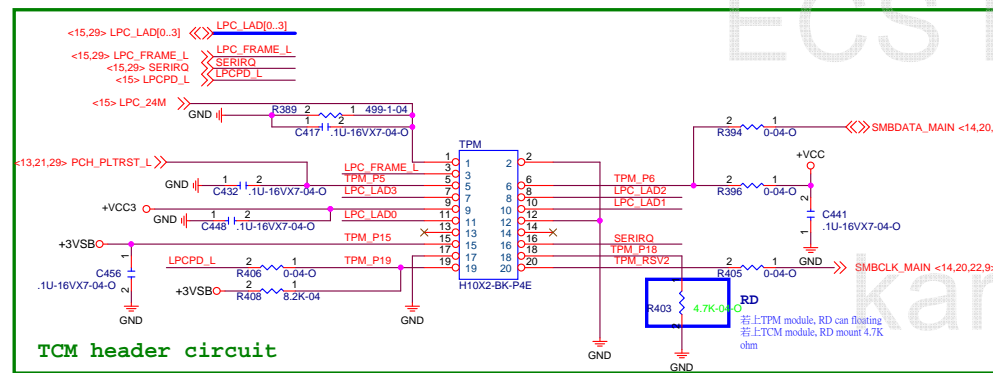
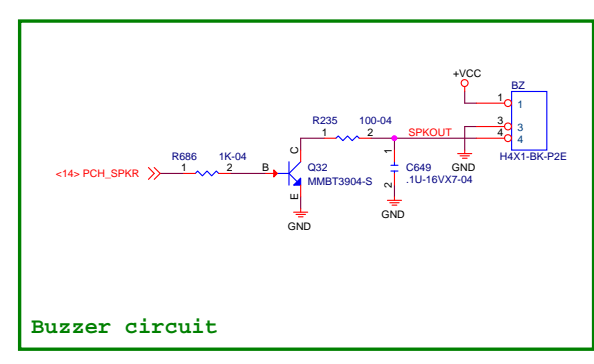
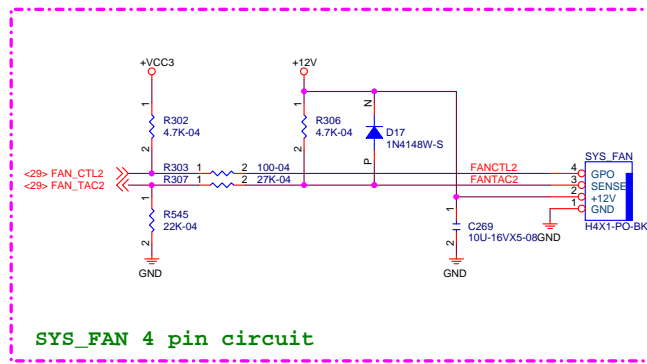
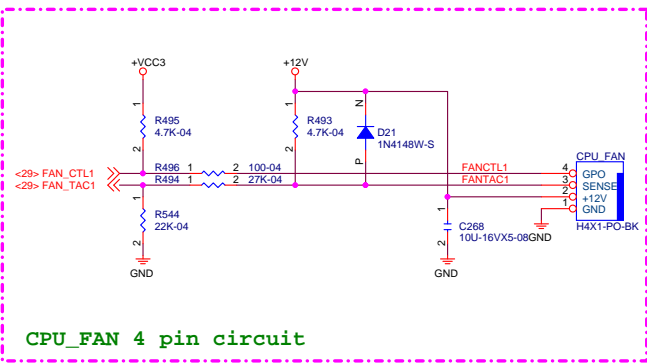
IT8625E 128-LQFP

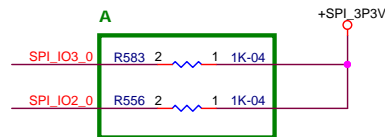
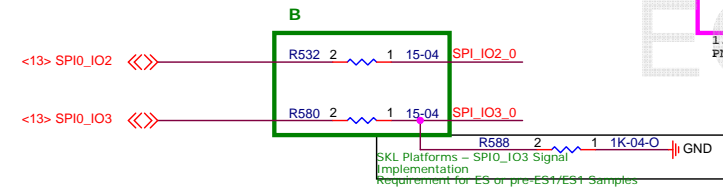
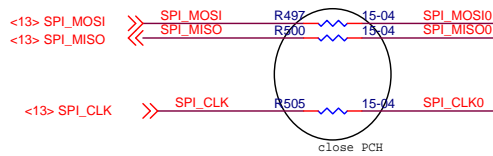


BIOS SELECTION



Elitegroup Computer Systems		
File	IT8625E	
Size	Document Number	H110M4-C43
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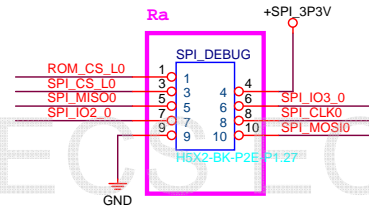
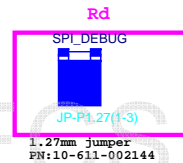
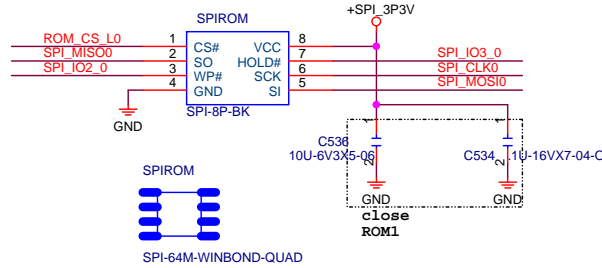




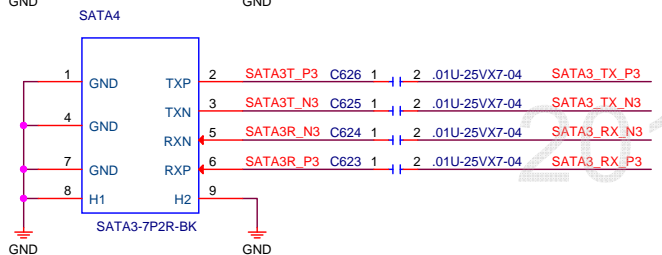
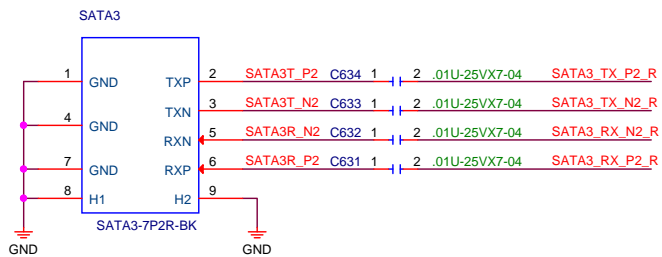
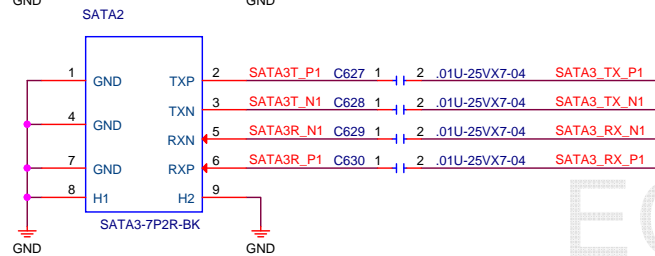
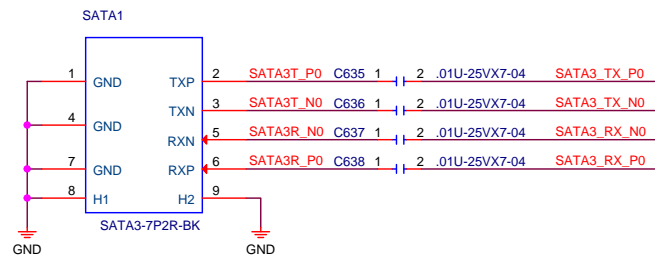
SPI mode selection:

MODE	BIOS WP	A	B
Standard/Dual	NA	10K	X
Quad	NA	1K	V

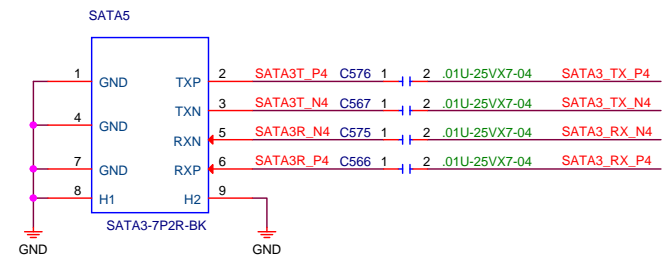
Note: Quad SPI not support WP



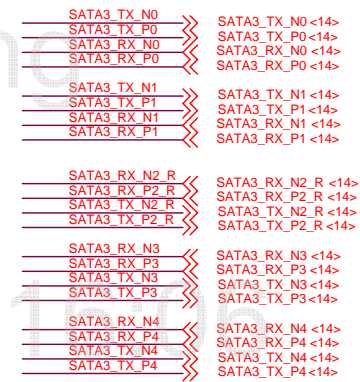
	Ra	Rd	Re
A3~A5	O	O	X
MP	X	X	O

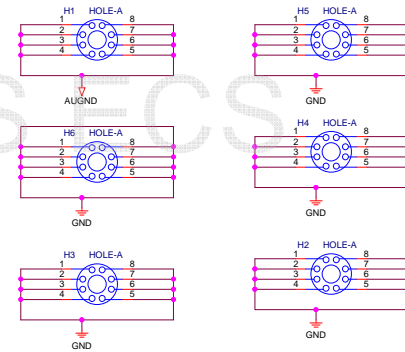
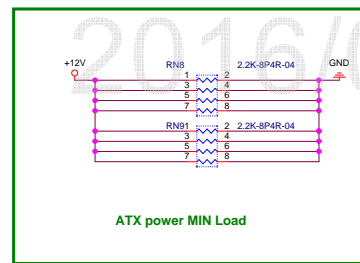
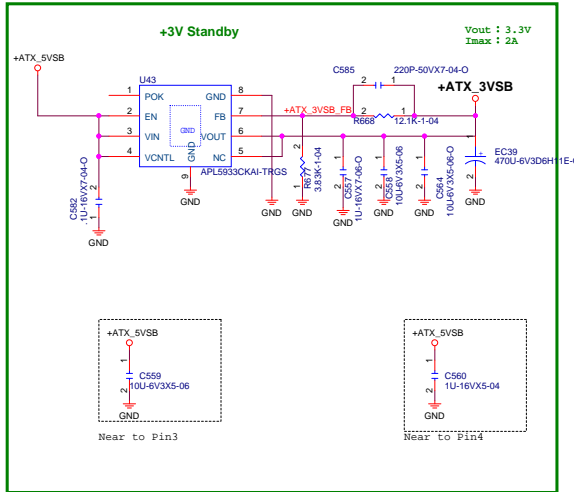
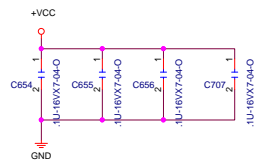
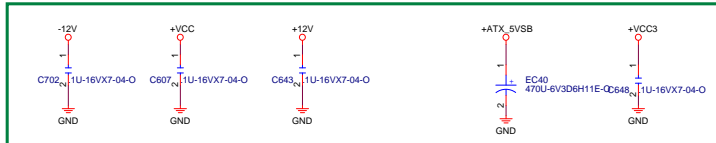
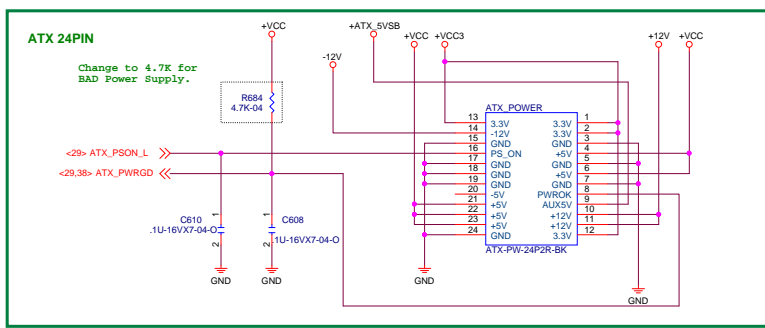


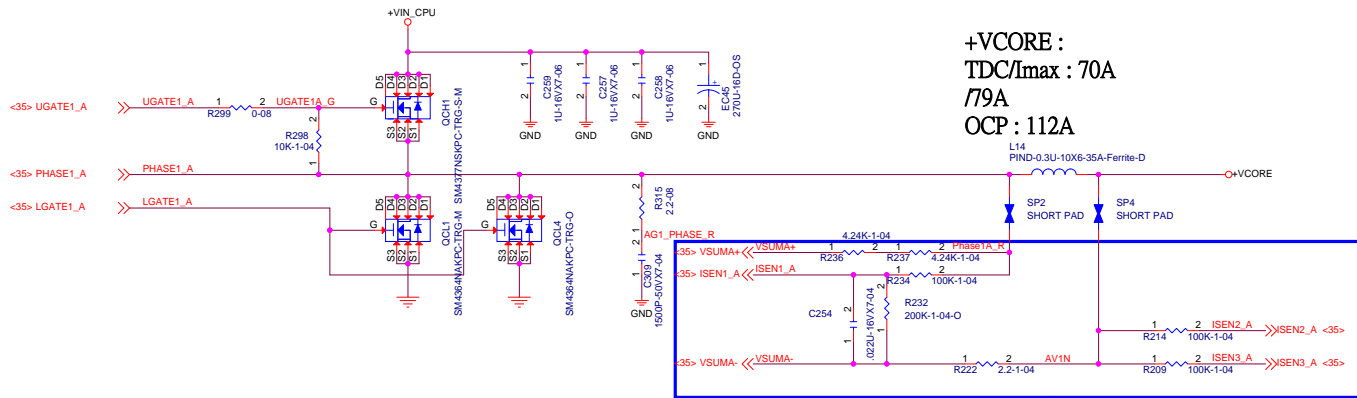
H110



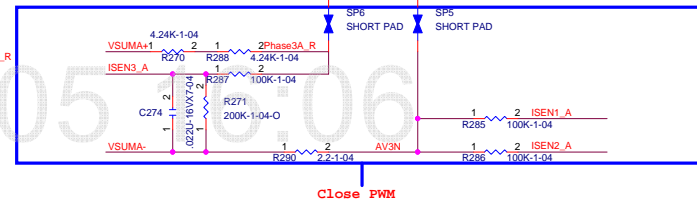
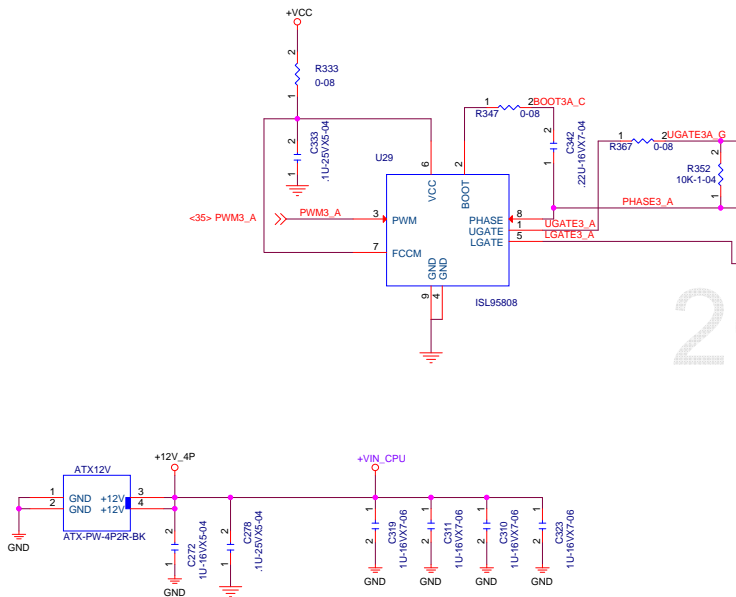
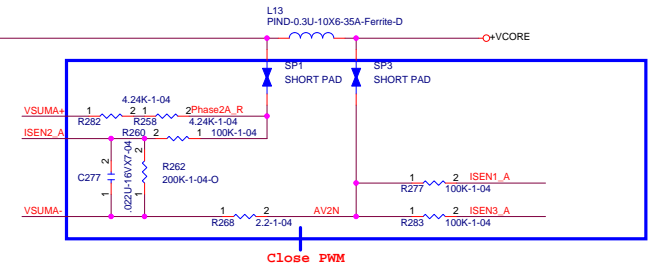
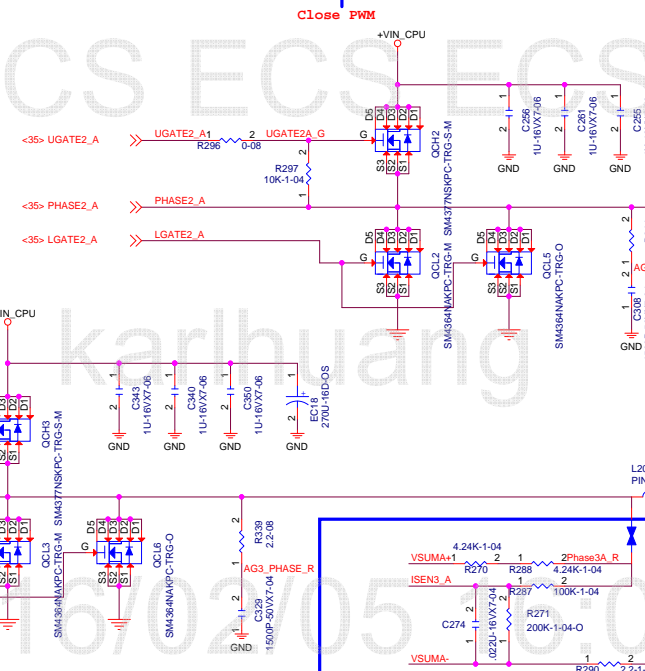
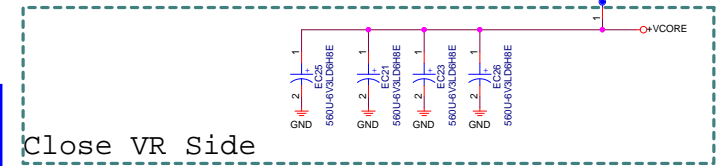
B150







+VCORE :
TDC/Imax : 70A
/79A
OCP : 112A



VCORE MOS MODULE PN
80-102-00100V MOSFET-M.CPU.SMD_3PHASE/HS*1/LS*1.SINOPower(4377/4364).HF.LEAD-FREE
03-052-837799 MOSFET-N-CH.SM4377NSKPC-TRG-.Vds=30V,Vgs=20V,Id=50A.Rds(on)=7m OHM.KPAK.....LEAD-FREE(RoHS/HF).SINOPower
03-053-436498 MOSFET-N-CH.SM4364NAKPC-TRG-.Vds=30V,Vgs=20V,Id=60A.Rds(on)=5.7m OHM.KPAK.....LEAD-FREE(RoHS/HF).SINOPower
80-102-00101D MOSFET-M.CPU.SMD_3PHASE/HS*1/LS*1.NIKO-SEM(516/618).HF.LEAD-FREE
03-052-851626 MOSFET-N-CH.PK516BA.Vds=30V,Vgs=20V,Id=51A.Rds(on)=7m OHM.POWERDFN5X6 8P.....LEAD-FREE(RoHS/HF).NIKO-SEM
03-052-861826 MOSFET-N-CH.PK618BA.Vds=30V,Vgs=20V,Id=59A.Rds(on)=5.5mOHM.POWERDFN5X6 8P.....HF.LEAD-FREE.NIKO-SEM

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+V CORE_GT :
TDC/Imax :
37A/51A
OCP : 70A

Close VR Side

VCCGT MOS MODULE PN
80D102-000285 MOSFET-M.MEMORY.SMD..1PHASE/HS*2LS*2..SINOPOWER/4377NS/4364NA..HF LEAD-FREE
03-052-837799 MOSFET N-CH.SM4377NSKPC-TRG..Vds=30V.Vgs=20V.Id=50A.Rds(on)=7m OHM.KPAK.....LEAD-FREE(RoHS/HF).SINOPOWER
03-053-436498 MOSFET N-CH.SM4364NAKPC-TRG..Vds=30V.Vgs=20V.Id=60A.Rds(on)=5.7m OHM.KPAK.....LEAD-FREE(RoHS/HF).SINOPOWER
80D102-000286 MOSFET-M.MEMORY.SMD..1PHASE/HS*2LS*2..NIKO-SEM/5168A/6188A..HF LEAD-FREE
03-052-851628 MOSFET N-CH.PK6188A..Vds=30V.Vgs=20V.Id=51A.Rds(on)=7m OHM.POWERDFN5X6 8P.....LEAD-FREE(RoHS/HF).NIKO-SEM
03-052-861826 MOSFET N-CH.PK6188A..Vds=30V.Vgs=20V.Id=59A.Rds(on)=5.5m OHM.POWERDFN5X6 8P.....LEAD-FREE(RoHS/HF).NIKO-SEM

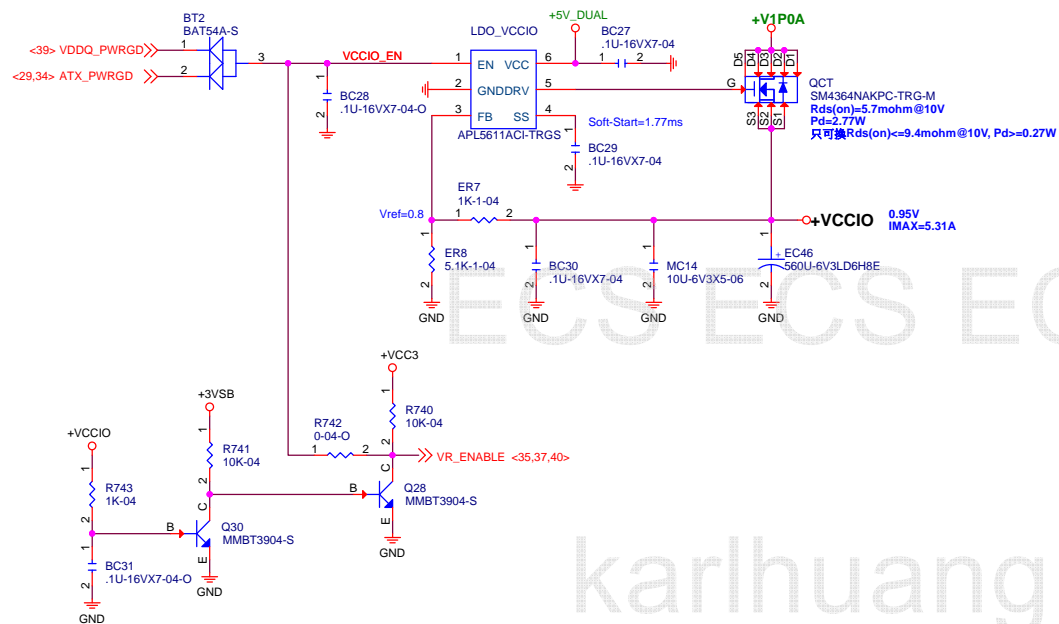
+VSA :1.05V
Imax : 11.1A
OCP : 33.33A

Close VR Side

$$V_{out} = (1 + R1/R2) \times 0.7$$

VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps

VCCSA MOS MODULE PN
80D102-00104Z MOSFET-M.CPU..SA.SMD..1PHASE/HS*1LS*1..SINOPOWER/4377NS/4364NA..HF LEAD-FREE
03-052-837799 MOSFET N-CH.SM4377NSKPC-TRG..Vds=30V.Vgs=20V.Id=50A.Rds(on)=7m OHM.KPAK.....LEAD-FREE(RoHS/HF).SINOPOWER
03-053-436498 MOSFET N-CH.SM4364NAKPC-TRG..Vds=30V.Vgs=20V.Id=60A.Rds(on)=5.7m OHM.KPAK.....LEAD-FREE(RoHS/HF).SINOPOWER
80D102-00105A MOSFET-M.CPU..SA.SMD..1PHASE/HS*1LS*1..NIKO-SEM/5168A/6188A..HF LEAD-FREE
03-052-851628 MOSFET N-CH.PK6188A..Vds=30V.Vgs=20V.Id=51A.Rds(on)=7m OHM.POWERDFN5X6 8P.....LEAD-FREE(RoHS/HF).NIKO-SEM
03-052-861826 MOSFET N-CH.PK6188A..Vds=30V.Vgs=20V.Id=59A.Rds(on)=5.5m OHM.POWERDFN5X6 8P.....HF LEAD-FREE.NIKO-SEM

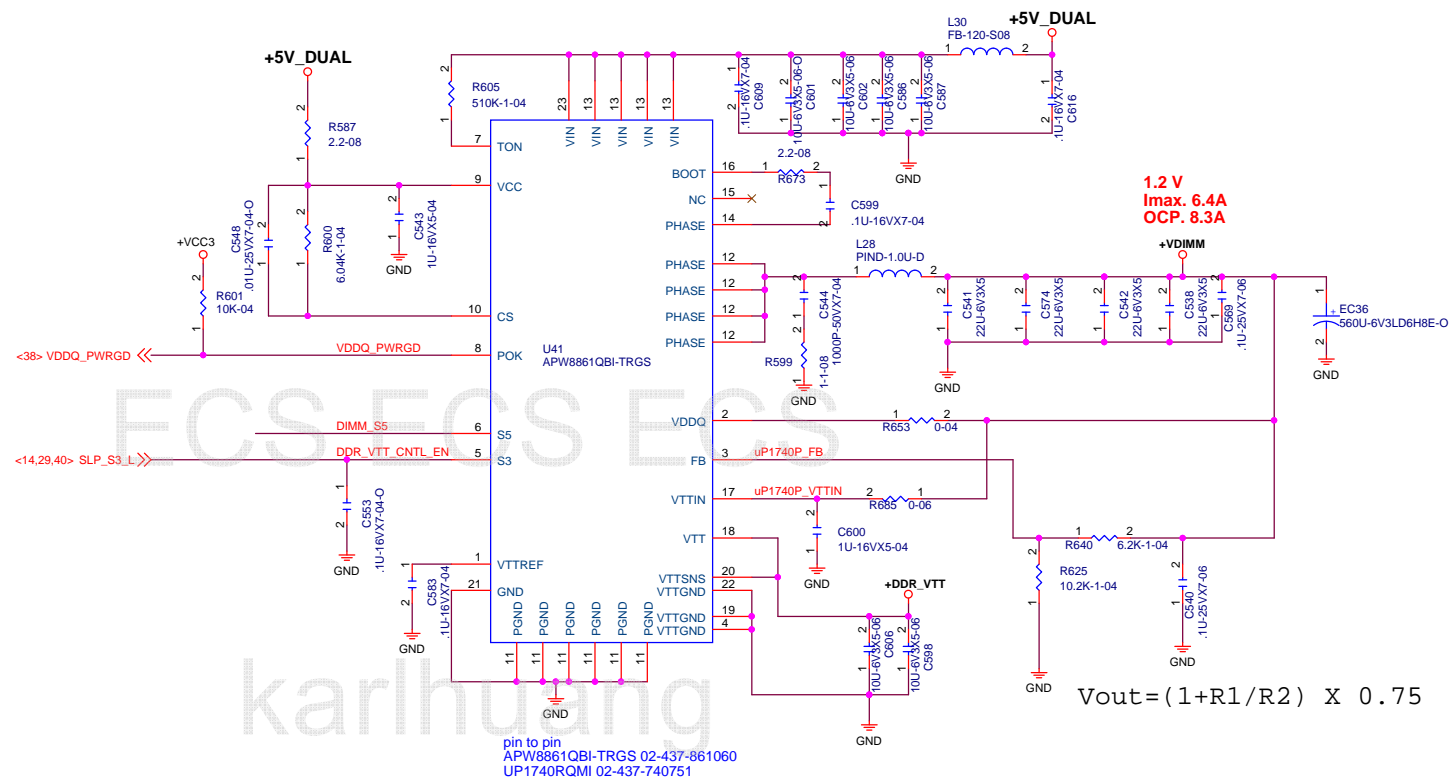
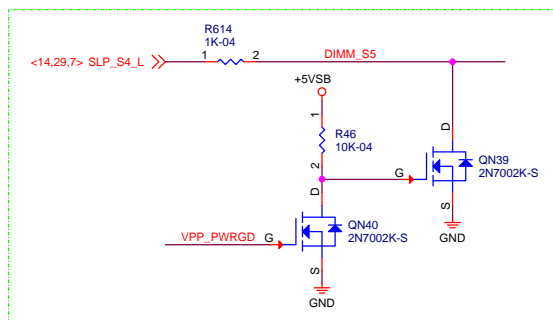


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VDIMM

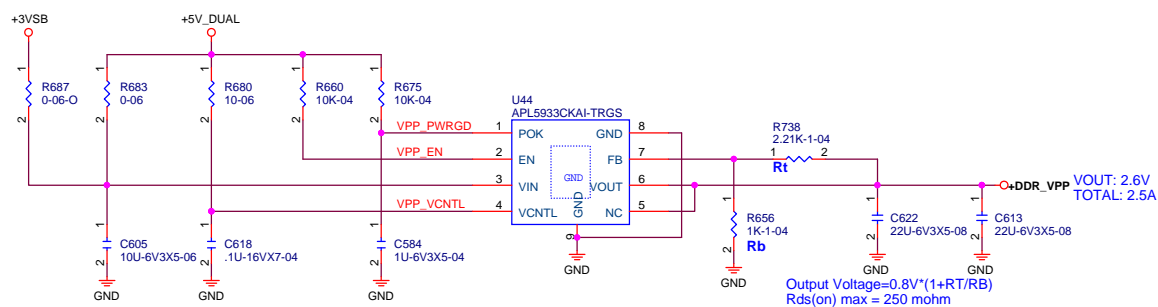
Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF

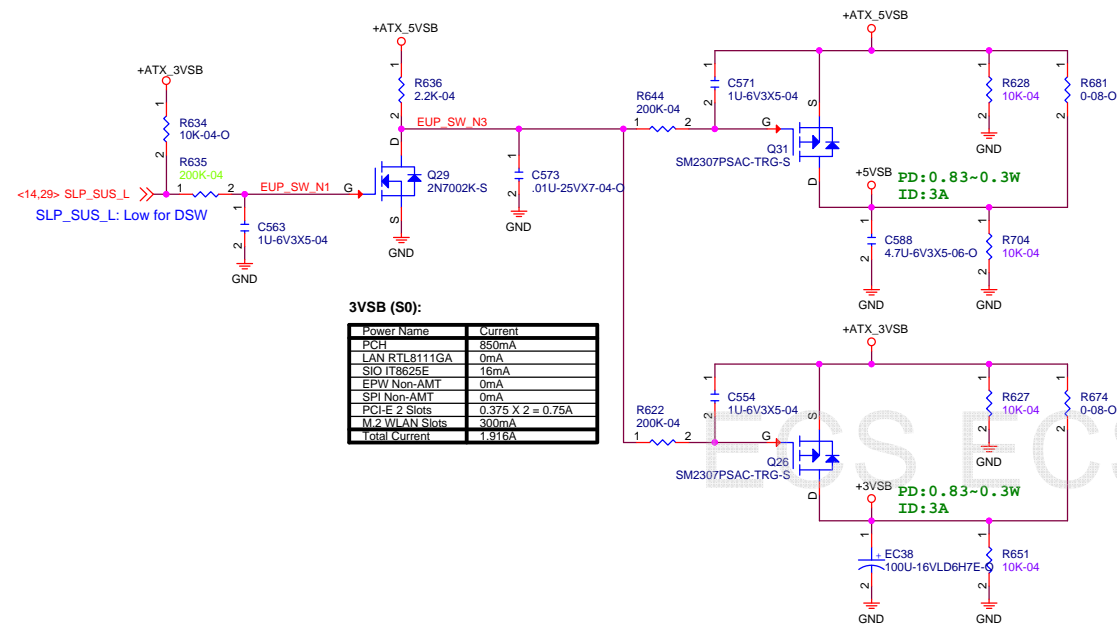


$$V_{out} = (1 + R_1/R_2) \times 0.75$$

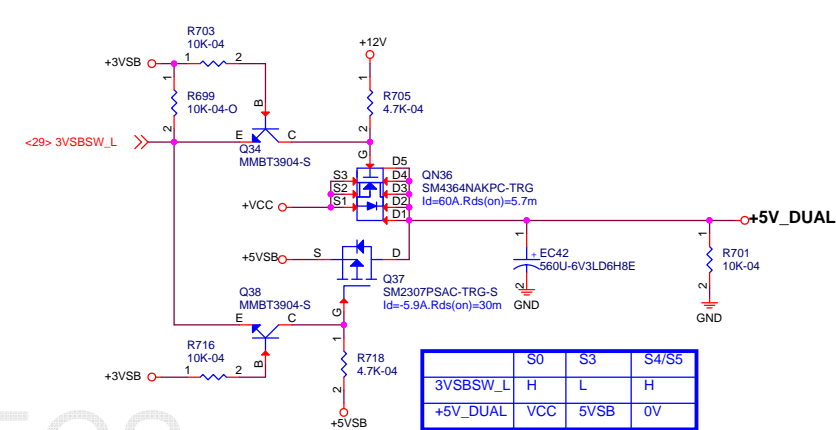
DDR_VPP



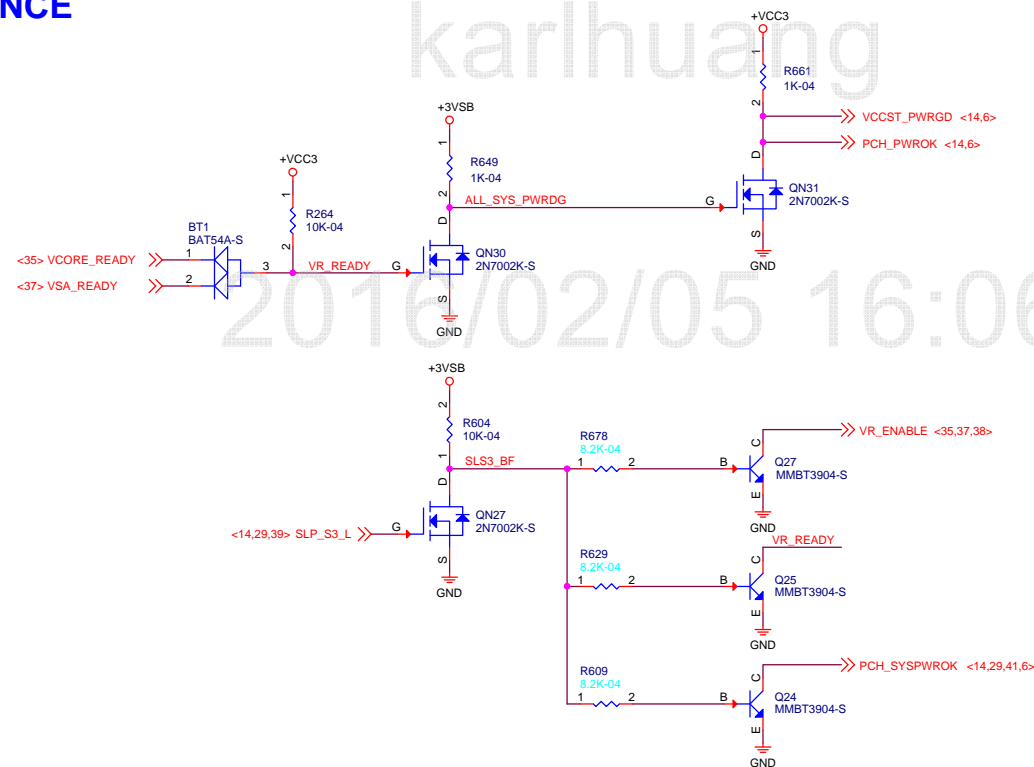
EuP Lot6 Power Saving Circuit



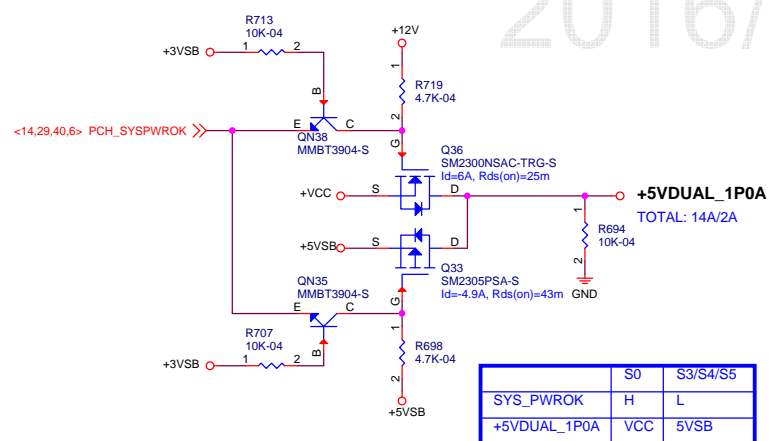
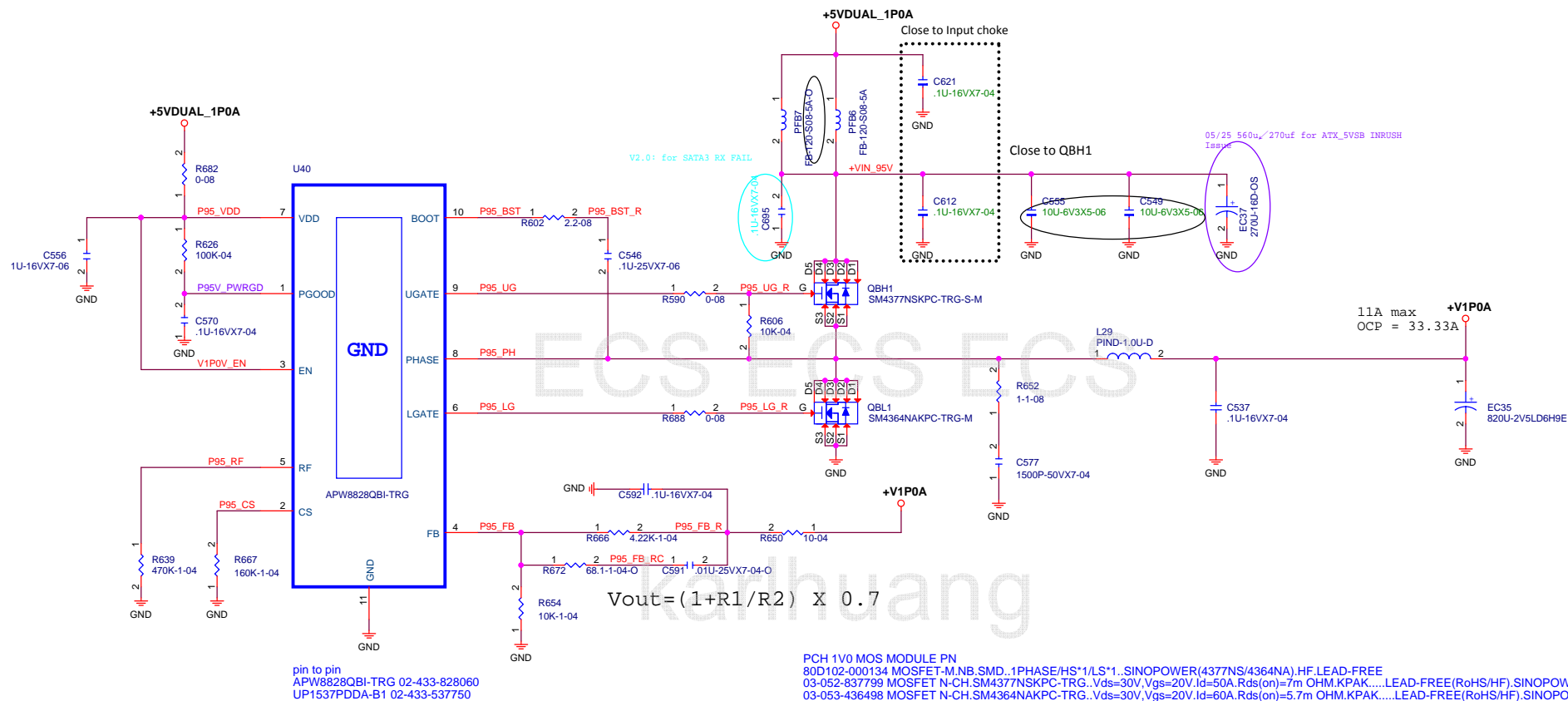
5VDUAL



POWER ON/DOWN SEQUENCE



V1P0A



	S0	S3/S4/S5
SYS_PWROK	H	L
+5VDUAL_1P0A	VCC	5VSB

Figure 41-2. SKL S Flow Diagram for RSMRST_PWRGD# Generation

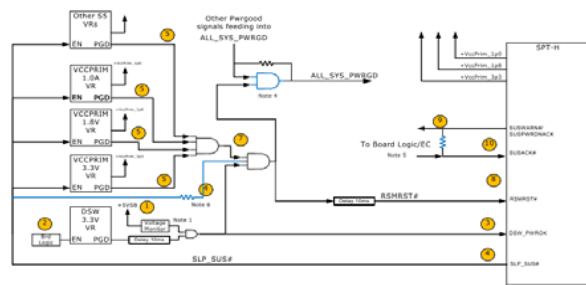


Figure 41-1. SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

